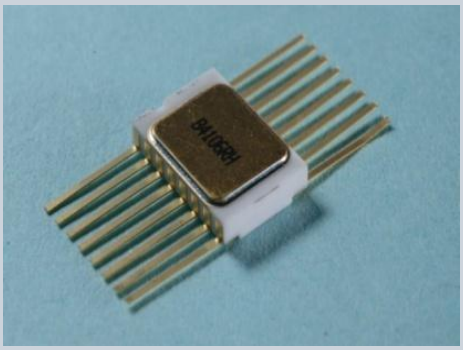
Ver 2.0

5.8GHz Radiation hardened wideband integer-N frequency synthesizer

Datasheet

Part Number：B4106RH



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Version No.	Publish Time	Revised Chapter	Revise Introduction	Note
1.0	2016/04/11		Initial Revision	
2.0	2018/07/23		Replace Template	

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1. Features

- **Scrubbing features**
  - Programmable dual-modulus prescaler: 8/9, 16/17, 32/33, 64/65
  - Programmable charge pump currents
  - Programmable antibacklash pulse width
  - 3-wire serial interface
  - Analog and digital lock detect
  - Hardware and software power-down mode
  - Pin compatible with ADF4108S
- **Electrical characteristics**
  - Supply voltage: 3.1V to 3.6V
  - RF input frequency range: 0.5GHz ~ 5.8GHz
  - Reference input frequency range: 20MHz ~ 300MHz
- **Reliability features**
  - Operating temperature: -55℃ ~ +125℃
  - ESD（human body model）: 2000V
  - Total ionizing dose: ≥100Krad（Si）
  - Single event latch-up threshold: ≥75MeV·cm^2/mg
  - Single event function interrupt: ≥10MeV cm^2/mg

2. General Description

The B4106RH frequency synthesizer can be used to implement local oscillators in the up-conversion and down-conversion sections of wireless receivers and transmitters. It consists of a low noise digital phase frequency detector (PFD), a precision charge pump (CP), a programmable reference divider, programmable A counter and B counter, and a dual-modulus prescaler (P/P + 1). The A (6-bit) counter and B (13-bit) counter, in conjunction with the dual-modulus prescaler (P/P + 1), implement an N divider (N = BP + A). In addition, the 14-bit reference counter (R Counter) allows selectable REF_{IN} frequencies at the PFD input. A complete phase-locked loop (PLL) can be implemented if the synthesizer is used with an external loop filter and voltage controlled oscillator (VCO). Its very high bandwidth means that frequency synthesizers can be eliminated in many high frequency systems, simplifying system architecture and reducing cost.

3. Function Block Diagram

B4106RH function block diagram is shown in figure 3-1.

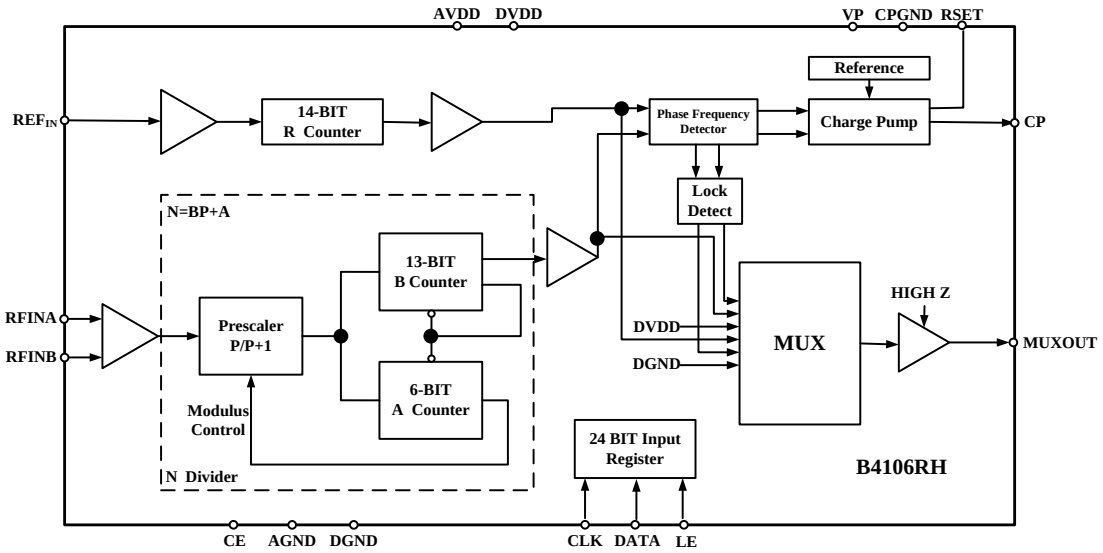


Figure 3-1 B4106RH function block digram

4. Package and Pin Functions Description

The provided package is: FP16.

B4106RH FP16 pin configuration is shown in figure 4-1, in top view the pin P1 is in the bottom of the left side, the pins are arranged in anticlockwise order.

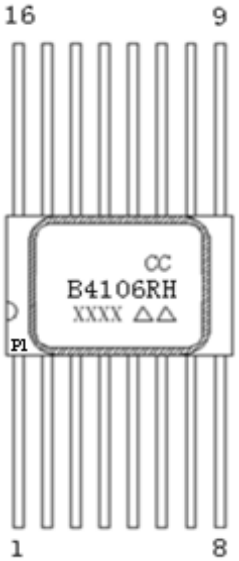


Figure 4-1 FP16 pin configuration

Talble 4-1 B4106RH Pin Function Descriptions

Pin No.	Pin Name	Pin Type	Function
1	R_{SET}	I/O	Bias for charge pump
2	CP	O	Charge pump output
3	CPGND	GND	Charge pump Ground
4	AGND	GND	Analog Ground
5	$RF_{IN}B$	I	Complementary Input to the RF Prescaler
6	$RF_{IN}A$	I	Input to the RF Prescaler
7	AV_{DD}	V_{DD}	Analog supply voltage
8	REF_{IN}	I	Reference Input
9	DGND	GND	Digital Ground
10	CE	I	Chip Enable
11	CLK	I	Serial Clock Input
12	DATA	I	Serial Data Input
13	LE	I	Load Enable
14	MUXOUT	O	Muxtiplexer Output
15	DV_{DD}	V_{DD}	Digital supply voltage
16	V_P	V_{DD}	Charge pump power supply

5. Detailed Description

5.1 Function Description

The main functions of B4106RH are as follows:

1) Reference input stage

The reference input stage is shown in figure 5-1. SW1 and SW2 are normally closed switches. SW3 is a normally open switch. When power-down is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that there is no loading of the REF_{IN} pin on power-down.

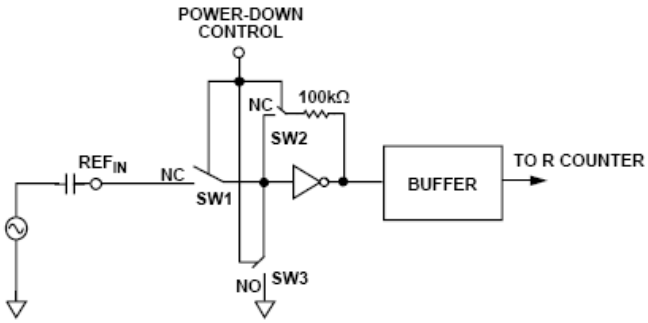


Figure 5-1 Reference input stage

2) RF input stage

The RF input stage is shown in figure 5-2. It is followed by a 2-stage limiting amplifier to generate the CML clock levels needed for the prescaler.

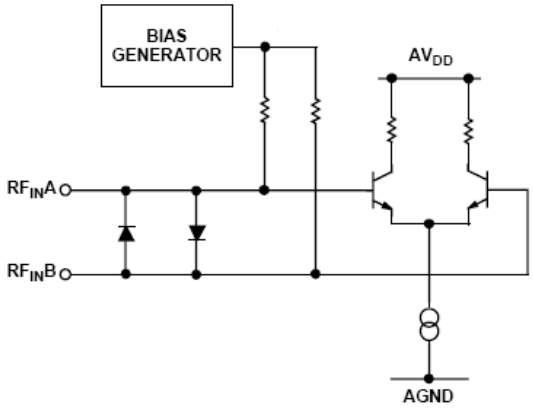


Figure 5-2 RF input stage

3) Prescaler (P/P+1)

The dual-modulus prescaler (P/P + 1), along with the A counter and B counter, enables the large division ratio, N, to be realized (N = BP + A). The dual-modulus prescaler, operating at CML levels, takes the clock from the RF input stage and divides it down to a manageable frequency for the CMOS A counter and B counter. The prescaler is programmable. It can be set in soft-ware to 8/9, 16/17, 32/33, or 64/65. It is based on a synchronous 4/5 core. There is a minimum divide ratio possible for fully contiguous output frequencies. This minimum is determined by P, the prescaler value, and is given by $(P^2 - P)$.

4) A counter and B counter

The A counter and B CMOS counter combine with the dual modulus prescaler to allow a wide ranging division ratio in the PLL feedback counter. The counters are specified to work when the prescaler output is 325 MHz or less. Thus, with an RF input frequency of 4.0 GHz, a prescaler value of 16/17 is valid, but a value of 8/9 is not valid.

Pulse swallow function

The A counter and B counter, in conjunction with the dual-modulus prescaler, make it possible to generate output frequencies that are spaced only by the reference frequency divided by R. The equation for the VCO frequency is

$$f_{VCO} = \left[\left(P \times B \right) + A \right] \times \frac{f_{REFIN}}{R}$$

where:

f_{VCO} is the output frequency of the external voltage controlled oscillator (VCO).

P is the preset modulus of the dual-modulus prescaler (8/9, 16/17, etc.).

B is the preset divide ratio of the binary 13-bit counter (3 to 8191).

A is the preset divide ratio of the binary 6-bit swallow counter (0 to 63).

f_{REFIN} is the external reference frequency oscillator.

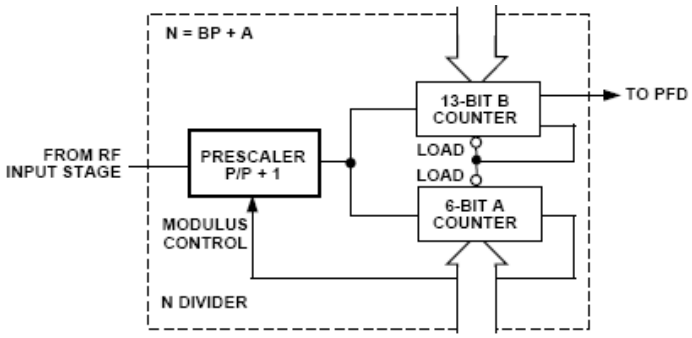


Figure 5-3 A counter and B counter

5) R counter

The 14-bit R counter allows the input reference frequency to be divided down to produce the reference clock to the phase frequency detector (PFD). Division ratios from 1 to 16,383 are allowed.

6) Phase frequency detector (PFD) and charge pump

The PFD takes inputs from the R counter and N counter (N = BP + A) and produces an output proportional to the phase and frequency difference between them. Figure 5-4 is a simplified schematic. The PFD includes a programmable delay element that controls the width of the antibacklash pulse. This pulse ensures that there is no dead zone in the PFD transfer function and minimizes phase noise and reference spurs. Two bits in the reference counter latch, ABP2 and ABP1, control the width of the pulse. See Table 5-3.

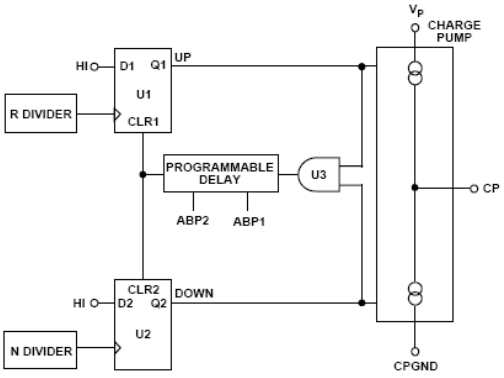


Figure 5-4 PFD simplified schematic

7) MUXOUT and lock detect

The output multiplexer on the B4106RH allows the user to access various internal points on the chip. The state of MUXOUT is controlled by M3, M2, and M1 in the function latch. Table 5-5 shows the full truth table. Figure 5-5 shows the MUXOUT section in block diagram form.

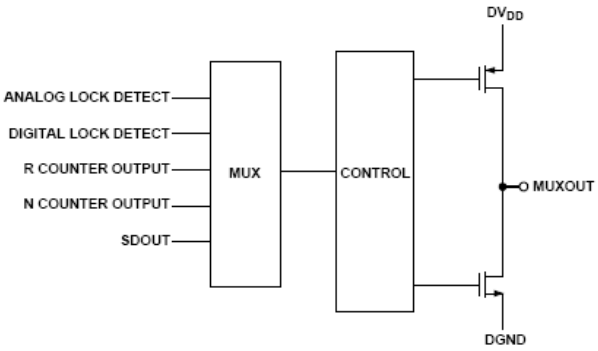


Figure 5-5 MUXOUT circuit

Lock detect

MUXOUT can be programmed for two types of lock detect: digital lock detect and analog lock detect.

Digital lock detect is active high. When LDP in the R counter latch is set to 0, digital lock detect is set high when the phase error on three consecutive phase detector cycles is less than 15 ns. With LDP set to 1, five consecutive cycles of less than 15 ns are required to set the lock detect. It stays set high until a phase error of greater than 25 ns is detected on any subsequent PFD cycle. The N-channel, open-drain, analog lock detect should be operated with an external pull-up resistor of 10 kΩ nominal. When lock is detected, this output is high with narrow, low-going pulses.

Caution: It is necessary to declare that, the MUXOUT output is used to test whether the circuit inside the chip is working correctly or not, and this port should be set to “Three-State Output” to ensure the correct work of the frequency synthesizer.

Otherwise, when MUXOUT is setted to “R Divider Output”、or “N Divider Output”，the phase noise at the radio frequency output port of frequency synthesizer may deteriorate and the frequency synthesizer is likely to fail to lock at a high output frequency.

8) Input shift register

The B4106RH digital section includes a 24-bit input shift register, a 14-bit R counter, and a 19-bit N counter, comprising a 6-bit A counter and a 13-bit B counter. Data is clocked into the 24-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of four latches on the rising edge of LE. The destination latch is determined by the state of the two control bits (C2, C1) in the shift register. These are the two LSBs, DB1 and DB0, as shown in the timing diagram of Figure 6-1. The truth table for theses bits is shown in Table 5-1. Table 5-2 shows a summary of how the latches are programmed.

Table 5-1 C1, C2 truth table

Control Bits		Data Latch
C2	C1	
0	0	R Counter
0	1	N Counter (A and B)
1	0	Function Latch (Including Prescaler)
1	1	Initialization Latch

Table 5-2 Latch Summary

REFERENCE COUNTER LATCH

RESERVED			LOCK DETECT	TEST MODE BITS		ANTIBACKLASH WIDTH		14-BIT REFERENCE COUNTER													CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	0	0	LDP	T2	T1	ABP2	ABP1	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2(0)	C1(0)

N COUNTER LATCH

RESERVED		CP GAIN	13-BIT B COUNTER													6-BIT A COUNTER						CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	X	G1	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A6	A5	A4	A3	A2	A1	C2(0)	C1(0)

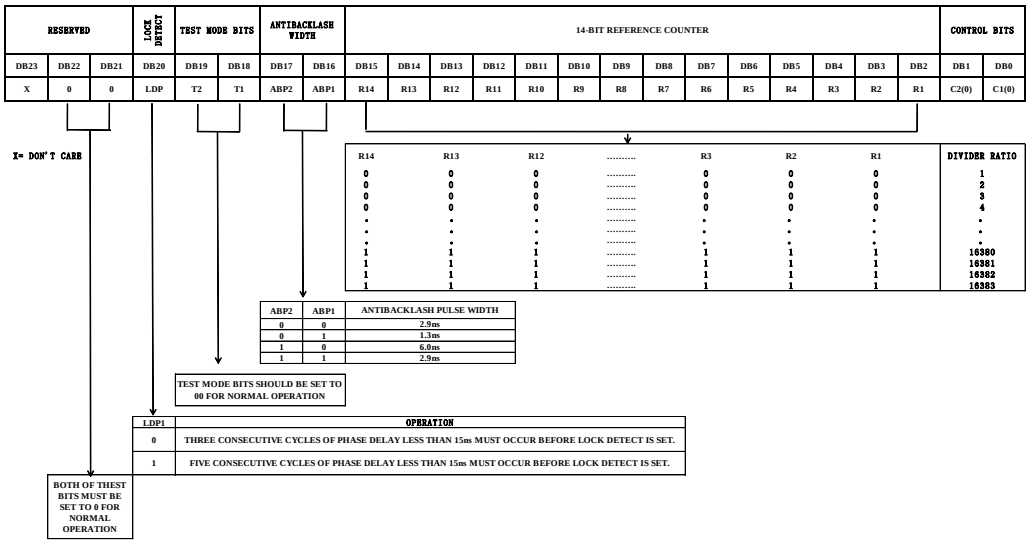
FUNCTION LATCH

PRESCALER VALUE		POWER-DOWN 2	CURRENT SETTING 2			CURRENT SETTING 1			TIMER COUNTER CONTROL				FASTLOCK MODE	FASTLOCK ENABLE	CP THREE-STATE	PPD POLARITY	MUXOUT CONTROL			POWER-DOWN 1	COUNTER RESET	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	CP16	CP15	CP14	CP13	CP12	CP11	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2(0)	C1(0)

INITIALIZATION LATCH

PRESCALER VALUE		POWER-DOWN 2	CURRENT SETTING 2			CURRENT SETTING 1			TIMER COUNTER CONTROL				FASTLOCK MODE	FASTLOCK ENABLE	CP THREE-STATE	PPD POLARITY	MUXOUT CONTROL			POWER-DOWN 1	COUNTER RESET	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	CP16	CP15	CP14	CP13	CP12	CP11	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2(0)	C1(0)

Table 5-3 Reference Counter Latch Map



RESERVED			LOCK DETECT	TEST MODE BITS		ANTIBACKLASH WIDTH		14-BIT REFERENCE COUNTER												CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	0	0	LDP	T2	T1	ABP2	ABP1	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2(0)	C1(0)

X= DON'T CARE

BOTH OF THEST BITS MUST BE SET TO 0 FOR NORMAL OPERATION

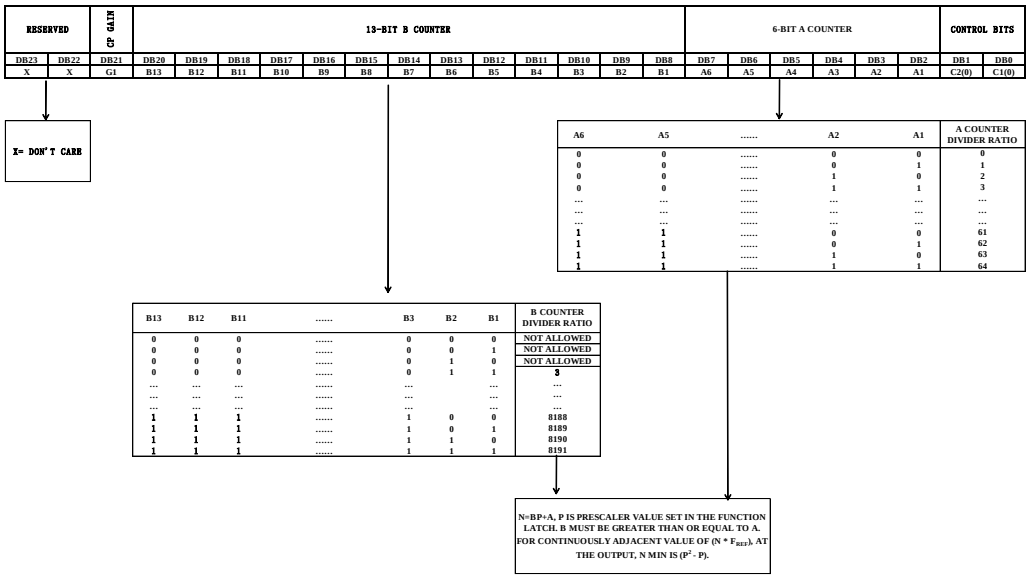
R14	R13	R12	.....	R3	R2	R1	DIVIDER RATIO
0	0	0	.....	0	0	0	1
0	0	0	.....	0	0	0	2
0	0	0	.....	0	0	0	3
0	0	0	.....	0	0	0	4
•	•	•	.....	•	•	•	•
•	•	•	.....	•	•	•	•
•	•	•	.....	•	•	•	•
1	1	1	.....	1	1	1	16380
1	1	1	.....	1	1	1	16381
1	1	1	.....	1	1	1	16382
1	1	1	.....	1	1	1	16383

ABP2	ABP1	ANTIBACKLASH PULSE WIDTH
0	0	2.9ns
0	1	1.3ns
1	0	6.0ns
1	1	2.9ns

TEST MODE BITS SHOULD BE SET TO 00 FOR NORMAL OPERATION

LDP1	OPERATION
0	THREE CONSECUTIVE CYCLES OF PHASE DELAY LESS THAN 15ns MUST OCCUR BEFORE LOCK DETECT IS SET.
1	FIVE CONSECUTIVE CYCLES OF PHASE DELAY LESS THAN 15ns MUST OCCUR BEFORE LOCK DETECT IS SET.

Table 5-4 N(A, B) Counter Latch Map



RESERVED		CP GAIN	13-BIT B COUNTER												6-BIT A COUNTER						CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	X	G1	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A6	A5	A4	A3	A2	A1	C2(0)	C1(0)

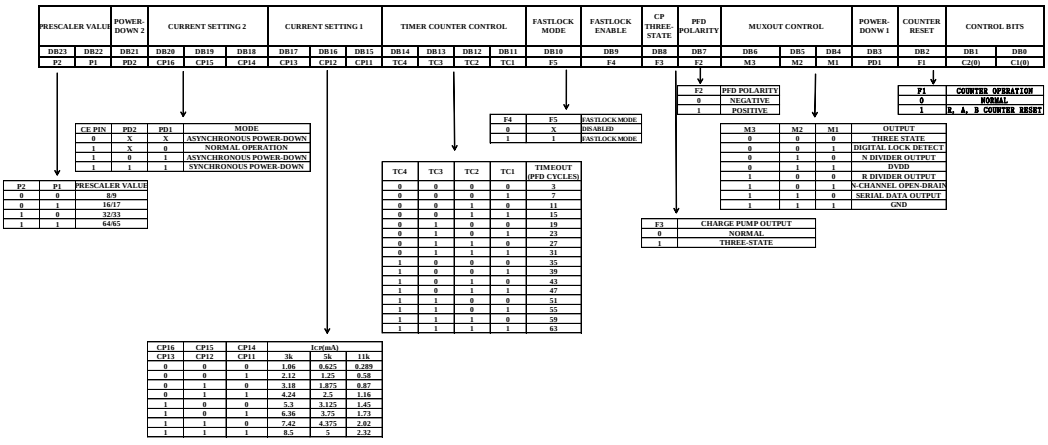
X= DON'T CARE

A6	A5	.....	A2	A1	A COUNTER DIVIDER RATIO
0	0	.....	0	0	0
0	0	.....	0	1	1
0	0	.....	1	0	2
0	0	.....	1	1	3
...	...	.....	...	...	...
...	...	.....	...	...	...
...	...	.....	...	...	...
1	1	.....	0	0	61
1	1	.....	0	1	62
1	1	.....	1	0	63
1	1	.....	1	1	64

B13	B12	B11	.....	B3	B2	B1	B COUNTER DIVIDER RATIO
0	0	0	.....	0	0	0	NOT ALLOWED
0	0	0	.....	0	0	1	NOT ALLOWED
0	0	0	.....	0	1	0	NOT ALLOWED
0	0	0	.....	0	1	1	3
...	...	...	.....	...		...	...
...	...	...	.....	...		...	...
...	...	...	.....	...		...	...
1	1	1	.....	1	0	0	8188
1	1	1	.....	1	0	1	8189
1	1	1	.....	1	1	0	8190
1	1	1	.....	1	1	1	8191

N=BP+A, P IS PRESCALER VALUE SET IN THE FUNCTION LATCH. B MUST BE GREATER THAN OR EQUAL TO A. FOR CONTINUOUSLY ADJACENT VALUE OF (N * F_{RFIN}), AT THE OUTPUT, N MIN IS (P^2 - P).

Table 5-5 Function Latch Map



PRESCALER VALUE		POWER-DOWN 2	CURRENT SETTING 2			CURRENT SETTING 1			TIMER COUNTER CONTROL				FASTLOCK MODE	FASTLOCK ENABLE	CP THREE-STATE	PFD POLARITY	MUXOUT CONTROL			POWER-DONW 1	COUNTER RESET	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	CP16	CP15	CP14	CP13	CP12	CP11	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2(0)	C1(0)

P2	P1	PRESCALER VALUE
0	0	8/9
0	1	16/17
1	0	32/33
1	1	64/65

CE PIN	PD2	PD1	MODE
0	X	X	ASYNCHRONOUS POWER-DOWN
1	X	0	NORMAL OPERATION
1	0	1	ASYNCHRONOUS POWER-DOWN
1	1	1	SYNCHRONOUS POWER-DOWN

F4	F5	FASTLOCK MODE
0	X	DISABLED
1	1	FASTLOCK MODE

TC4	TC3	TC2	TC1	TIMEOUT (PFD CYCLES)
0	0	0	0	3
0	0	0	1	7
0	0	1	0	11
0	0	1	1	15
0	1	0	0	19
0	1	0	1	23
0	1	1	0	27
0	1	1	1	31
1	0	0	0	35
1	0	0	1	39
1	0	1	0	43
1	0	1	1	47
1	1	0	0	51
1	1	0	1	55
1	1	1	0	59
1	1	1	1	63

F2	PFD POLARITY
0	NEGATIVE
1	POSITIVE

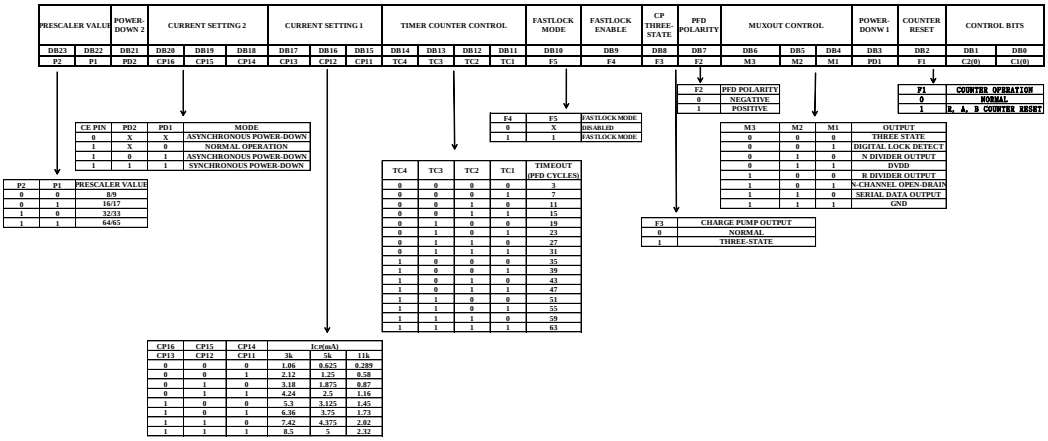
F3	CHARGE PUMP OUTPUT
0	NORMAL
1	THREE-STATE

M3	M2	M1	OUTPUT
0	0	0	THREE STATE
0	0	1	DIGITAL LOCK DETECT
0	1	0	N DIVIDER OUTPUT
0	1	1	DVDD
1	0	0	R DIVIDER OUTPUT
1	0	1	N-CHANNEL OPEN-DRAIN
1	1	0	SERIAL DATA OUTPUT
1	1	1	GND

F1	COUNTER OPERATION
0	NORMAL
1	R, A, B COUNTER RESET

CP16	CP15	CP14	Icp(mA)		
CP13	CP12	CP11	3k	5k	11k
0	0	0	1.06	0.625	0.289
0	0	1	2.12	1.25	0.58
0	1	0	3.18	1.875	0.87
0	1	1	4.24	2.5	1.16
1	0	0	5.3	3.125	1.45
1	0	1	6.36	3.75	1.73
1	1	0	7.42	4.375	2.02
1	1	1	8.5	5	2.32

Table 5-6 Initialization Latch Map



9) The function latch

With C2 and C1 set to 1 and 0, respectively, the on-chip function latch is programmed. Table 5-5 shows the input data format for programming the function latch.

Counter Reset

DB2 (F1) is the counter reset bit. When this is 1, the R counter and the N (A, B) counter are reset. For normal operation, this bit should be 0. When powering up, disable the F1 bit (set to 0). The N counter will then resume counting in close alignment with the R counter. (The maximum error is one prescaler cycle).

Power-Down

DB3 (PD1) and DB21 (PD2) provide programmable power-down modes. They are enabled by the CE pin.

When the CE pin is low, the device is immediately disabled regardless of the states of PD2, PD1.

In the programmed asynchronous power-down, the device powers down immediately after latching 1 into the PD1 bit, with the condition PD2 is loaded with 0.

In the programmed synchronous power-down, the device power-down is gated by the charge pump to prevent unwanted frequency jumps. Once the power-down is enabled by writing 1 into the PD1 bit (provided that 1 has also been loaded to PD2), then the device goes into power-down during the next charge pump event.

When a power-down is activated (either synchronous or asynchronous mode, including CE pin activated power-down), the following events occur:

• All active dc current paths are removed.

• The R, N, and timeout counters are forced to their load state conditions.

• The charge pump is forced into three-state mode.

• The digital clock detect circuitry is reset.

• The RF_{IN} input is debiased.

• The reference input buffer circuitry is disabled.

• The input register remains active and capable of loading and latching data.

MUXOUT Control

The on-chip multiplexer is controlled by M3, M2, and M1 on the B4106RH family. Table 5-5 shows the truth table.

Fastlock Enable Bit

DB9 and DB10 of the function latch are the fastlock enable bits. When this bits is 11, and CP Gain bit is 1, fastlock is enabled.

Timer Counter Control

The user has the option of programming two charge pump currents. The intent is that Current Setting 1 is used when the RF output is stable and the system is in a static state. Current Setting 2 is used when the system is dynamic and in a state of change (that is, when a new output frequency is programmed). The normal sequence of events follows.

The user initially decides what the preferred charge pump currents are going to be. For example, the choice may be 2.5 mA as Current Setting 1 and 5 mA as the Current Setting 2.

Simultaneously, the decision must be made as to how long the secondary current stays active before reverting to the primary current. This is controlled by the timer counter control bits, DB14 to DB11 (TC4 to TC1), in the function latch. The truth table is given in Table 5-5.

To program a new output frequency, simply program the N (A, B) counter latch with new values for A and B. Simultaneously, the CP gain bit can be set to 1, which sets the charge pump with the value in CPI6 to CPI4 for a period of time determined by TC4 to TC1. When this time is up, the charge pump current reverts to the value set by CPI3 to CPI1. At the same time, the CP gain bit in the N (A, B) counter latch is reset to 0 and is now ready for the next time the user wishes to change the frequency.

Note that there is an enable feature on the timer counter. It is enabled when Fastlock Mode 2 is chosen by setting the fastlock mode bit (DB10) in the function latch to 1.

Charge Pump Currents

CPI3, CPI2, and CPI1 program Current Setting 1 for the charge pump. CPI6, CPI5, and CPI4 program Current Setting 2 for the charge pump. The truth table is

given in Table 5-5.

Prescaler Value

P2 and P1 in the function latch set the prescaler values. The prescaler value should be chosen so that the prescaler output frequency is always less than or equal to 325 MHz. Therefore, with an RF frequency of 4 GHz, a prescaler value of 16/17 is valid, but a value of 8/9 is not valid.

PD Polarity

This bit sets the phase detector polarity bit. See Table 5-5.

CP Three-State

This bit controls the CP output pin. With the bit set high, the CP output is put into three-state. With the bit set low, the CP output is enabled.

10) The initialization latch

When C2 and C1 = 1 and 1, respectively, the initialization latch is programmed. This is essentially the same as the function latch (programmed when C2 and C1 = 1 and 0, respectively).

However, when the initialization latch is programmed, there is an additional internal reset pulse applied to the R and N (A, B) counters. This pulse ensures that the N (A, B) counter is at the load point when the N (A, B) counter data is latched and the device begins counting in close phase alignment.

If the latch is programmed for synchronous power-down (CE pin is high, PD1 bit is high, and PD2 bit is low), the internal pulse also triggers this power-down. The prescaler reference and the oscillator input buffer are unaffected by the internal reset pulse; therefore, close phase alignment is maintained when counting resumes.

When the first N (A, B) counter data is latched after initialization, the internal reset pulse is again activated. However, successive N (A, B) counter loads after this will not trigger the internal reset pulse.

Device Programming After Initial Power-Up

After initial power up of the device, there are three methods for programming the device: initialization latch, CE pin, and counter reset.

Initialization Latch Method

• Apply V_{DD}.

• Program the initialization latch (11 in two LSBs of input word). Make sure that the F1 bit is programmed to 0.

• Do a function latch load (10 in two LSBs of the control word), making sure that the F1 bit is programmed to a 0.

• Do an R load (00 in two LSBs).

Do an N (A, B) load (01 in two LSBs).

When the initialization latch is loaded, the following occurs:

• The function latch contents are loaded.

• An internal pulse resets the R, N (A, B), and timeout counters to load-state conditions and also three-states the charge pump. Note that the prescaler band gap reference and the oscillator input buffer are unaffected by the internal reset pulse, allowing close phase alignment when counting resumes.

• Latching the first N (A, B) counter data after the initialization word activates the same internal reset pulse. Successive N (A, B) loads will not trigger the internal reset pulse, unless there is another initialization.

11) CE pin method

• Apply VDD.

• Bring CE low to put the device into power-down. This is an asychronous power-down in that it happens immediately.

• Program the function latch (10).

• Program the R counter latch (00).

• Program the N (A, B) counter latch (01).

• Bring CE high to take the device out of power-down. The R and N (A, B) counters now resume counting in close alignment.

Note that after CE goes high, a 1us duration may be required for the prescaler band gap voltage and oscillator input buffer bias to reach steady state.

CE can be used to power the device up and down to check for channel activity. The input register does not need to be reprogrammed each time the device is isabled and enabled as long as it is programmed at least once after VDD is initially applied.

12) Counter reset method

• Apply VDD.

• Do a function latch load (10 in two LSBs). As part of this, load 1 to the F1 bit. This enables the counter reset.

• Do an R counter load (00 in two LSBs).

• Do an N (A, B) counter load (01 in two LSBs).

• Do a function latch load (10 in two LSBs). As part of this, load 0 to the F1 bit. This disables the counter reset.

This sequence provides the same close alignment as the initialization method. It offers direct control over the internal reset. Note that counter reset holds the counters

at load point and three-states the charge pump but does not trigger synchronous power-down.

5.2 Storage Condition

Packaged product should be stored in the ventilate warehouse with ambient temperature 10℃～30℃ and relative humidity less than 70%. There should be no acid, alkali or other radiant gas in the environment.

5.3 Absolute Maximum Ratings

a) Supply voltage（AV_{DD}、DV_{DD}、V_P）：-0.3V ～ 3.9V
b) Voltage on any input（V_I）：-0.3 V ～ V_{DD}+0.3V
c) Operation temperature range（T_A）：-55℃ ~125℃
d) Storage temperature range（T_{stg}）：-65℃ ～ 150℃
e) Maximum Junction Temperature（T_J）：175℃
f) Thermal resistance（$R_{th(J-C)}$）：12.5℃/W
g) Lead Temperature 10s（T_H）：260℃

5.4 Recommended Operation Conditions

a) Supply voltage (AV_{DD}、DV_{DD}、V_P) : 3.1V ~ 3.6V
b) Operation temperature range(T_A) :- 55℃ ~ 125℃

6. Specifications

All electrical characteristics are shown in table 6-1. AV_{DD} = DV_{DD} = V_P =3.1V to 3.6V, AGND = DGND = CPGND = 0 V, R_{SET} = 5.1 kΩ, dBm referred to 50 Ω, T_A = -55 ℃ to 125 ℃, unless otherwise noted.

Table 6-1 B4106RH electrical characteristics

Parameter	Min.	Typ.	Max.	Unit	Test conditions/comments
RF CHARACTERISTICS					
RF Input Frequency(RF_{IN})[1]	0.5		5.8	GHz	For lower frequencies, ensure slew rate (SR) > 320V/μS
RF Input Sensitivity	-5		5	dBm	

Maximum Allowable			300	MHz	P=8
Prescaler Output Frequency			325	MHz	P=16
REF_{IN} CHARACTERISTICS					
REF_{IN} Input Frequency[1]	20		300	MHz	For f < 20MHz,ensure SR > 50V/μS
REF_{IN} Input Sensitivity	0.8		V_{DD}	Vp-p	Biased at AV_{DD}/2.
REF_{IN} Input Capacitance			10	pF	
REF_{IN} Input Current			±100	μA	
PHASE DETECTOR					
Phase Detector Frequency			104	MHz	
CHARGE PUMP					
I_{CP} Sink/Source					
High Value		5		mA	With R_{SET}=5.1KΩ
Low Value		0.5		mA	
Absolute Accuracy		2.5		%	With R_{SET}=5.1KΩ
R_{SET} Range	3		11	KΩ	
I_{CP} Three-State Leakage		1		nA	1nA typical; T_A=25℃
Sink and Source Current Matching		2		%	0.5V ≤V_{CP}≤V_P-0.5V
I_{CP} vs. V_{CP}		1.5		%	0.5V ≤V_{CP}≤V_P-0.5V
I_{CP} vs. Temperature		2		%	V_{CP}= V_P/2
LOGIC INPUTS					
V_{IH}, Input High Voltage	1.5			V	
V_{IL}, Input Low Voltage			0.6	V	
I_{INH}, I_{INL}, Input Current			±1	μA	
C_{IN}, Input Capacitance			10	pF	
LOGIC OUTPUTS					
V_{OH}, Output High Voltage	1.4			V	Open-drain output chosen, 1 kΩ pull-up resistor to 1.8 V
V_{OH}, Output High Voltage	V_{DD}-0.4			V	CMOS output chosen, I_{OL}=-500μA
V_{OL}, Output Low Voltage			0.4	V	I_{OL}=500μA
I_{OH}, Output High Current			500	uA	
POWER SUPPLIES					
AV_{DD} ,DV_{DD}	3.1		3.6	V	AV_{DD}=DV_{DD}

V_P	AV_{DD}		3.6	V	$AV_{DD} \leq V_P$
$I_{DD}(AI_{DD}+ I_P)$			17	mA	$AV_{DD}=DV_{DD}=V_P=3.3V$；P=32；RF_{IN}=5.8GHz；f_{PFD}=200KHz；REF_{IN}=10MHz；R_{SET}=5.1KΩ
DI_{DD}			5	mA	
Power-Down Mode			200	μA	
NOISE CHARACTERISTICS					
Normalized Phase Noise Floor[2]		-219		dBc/Hz	
Normalized 1/f Noise[3]		-117		dBc/Hz	
Phase Noise Performance@VCO output					
5800MHz		-75		dBc/Hz	@1KHz offset and 1MHz PFD frequency
Spurious Signals					
5800MHz		-65		dBc	@1MHz and 1MHz PFD frequency

Note1. If the minimum reference frequency and the RF input frequency of B4106RH need to be less than 20MHz and 500MHz respectively, adding an additional clock buffer is necessary.

Note2. The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20 log N (where N = BP + A) and 10 log f_{PFD}. $PN_{SYNTH} = PN_{TOT} - 10 \log f_{PFD} - 20 \log N$.

Note3. The PLL phase noise is composed of 1/f (flicker) noise plus the normalized PLL noise floor. The formula for calculating the 1/f noise contribution at an RF frequency, f_{RF} and at a frequency offset, f, is given by $PN = PN_{1\_f} + 10\log(10KHz/f) + 20\log(f_{RF}/1GHz)$.

TIMING CHARACTERISITICS

$AV_{DD} = DV_{DD} = V_P$ =3.1V 至 3.6V, AGND = DGND = CPGND = 0 V, R_{SET} = 5.1 kΩ, dBm referred to 50 Ω, T_A = -55 ℃ to 125 ℃, unless otherwise noted.

Table 6-2 B4106RH timing characteristics

parameter	Limit	Unit	Test Conditions/comments
t_1	10	ns min	DATA to CLOCK Setup Time
t_2	10	ns min	DATA to CLOCK Hold Time
t_3	25	ns min	CLOCK High Duration
t_4	25	ns min	CLOCK Low Duration
t_5	10	ns min	CLOCK to LE Setup Time
t_6	20	ns min	LE Pulse Width

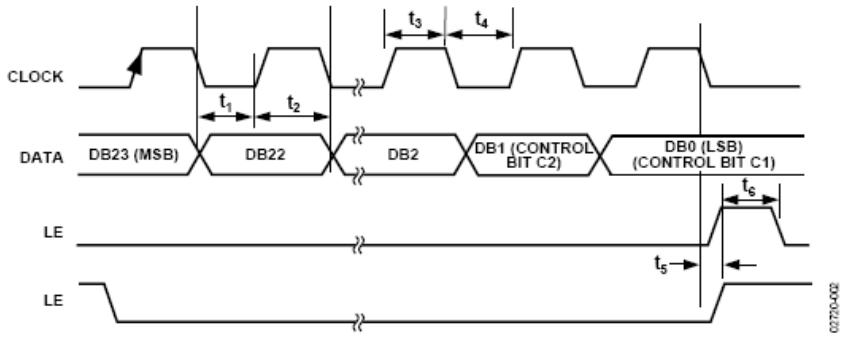


Figure 6-1 B4106RH timing diagram

7. Notice

1) The RF and REF input signals need sufficient slew rate at different operating frequencies to ensure the dividers work correctly (SR $\geqslant 2\times\pi\times f\times V_P$, f is the input frequency, V_P is the input amplitude). For example, when the input frequency f is 500MHz and the input amplitude V_P is 0dBm, the slew rate SR needs to be larger than 942V/us.

In addition, the RF input stage is differential input. If a single input is used in application, unused input must be grounded with a capacitor, and the value must be the same as the DC-blocking capacitor at the used input.

2) In application, if the user need to use the lock detect, it is recommended to use the digital lock detect. When the PFD frequency is high or low, if the digital lock detect does not work, analog lock detect can be used. However, it should be noted that using the lock detect may affect device performance and PLL stability.

3) Serial control signals can be generated by MCU, DSP or FPGA. The serial clock and data should be clean. Using FPGA should avoid the competitive adventure. If the competitive adventure is unavoidable, capacitors can be connected in parallel with the clock and data line to absorb glitch in the case of ensuring the driving ability.

4) The off-chip LPF directly affects the phase noise and lock time of the frequency synthesizer. In the case of low noise applications, the passive LPF is used to convert the charge pump output current into a control voltage usually. In the circuit design, it is recommended to use the third-order LPF to improve the suppression of spurious signals.

5) The MUXOUT port is only used to detect the internal signal state. When turned on, it may deteriorate the noise performance of the frequency synthesizer, and even cause the PLL to be loss of lock. When the PLL is working properly, the

MUXOUT port should be set to the three-state output.

6) In the space environment, the single-event effect may cause functional interruptions of the device and cannot be automatically recovered. When the MUXOUT output lock signal is low, the device needs to be reset through the CE port and refresh the register.

7) In application, the main characteristic parameters of the device, such as the PFD frequency, CP current and etc. should be designed and optimized with the characteristic parameters of off-chip VCO and LPF to ensure the frequency synthesizers work properly. And, the maximum RF frequency will be affected by testing condition, PCB, external devices, chip welding and etc. Therefore, working in the state of extreme frequencies is not suggested. It is recommended working in the state of below 5.5GHz to ensure the reliability and achieve the best performance.

8) The bandwidth of off-chip LPF is between one tenth and one fifteen of the PFD frequency. When PFD frequency is too high, the bandwidth is out of this range that may cause the PLL to be loss of lock. The PFD frequency should be designed properly in application.

9) The RF input port and off-chip VCO output port should be impedance matched and the connection of these ports should be designed as short as possible.

10) The ripple of the power supply voltage will affect the working state of the device. When the voltage ripple is too large, the device may be loss of lock. Therefore, it is recommended to use a low dropout regulator (LDO) as the power supply.

11) The power supply of the device, such as analog power supply (AV_{DD}), digital power supply (DV_{DD}) and CP power supply (V_P), should have good decoupling. Decoupling capacitors should be placed as close as possible to those pins.

8. Typical Application

The circuit diagram of B4106RH typical application is shown in figure 8-1. The reference input signal is applied to the circuit at $FREF_{IN}$ with a TCXO or another low noise frequency source. The third-order LPF output (The values of R and C are typical values in figure 8-1. That need to be optimized according to the condition of the PLL loop.) drives the VCO, which in turn is fed back to the RF input of the PLL synthesizer and also drives the RF output terminal. The MUXOUT pin can be programmed to monitor various internal signals in the synthesizer. One of these is the LD or lock-detect signal. The device has a simple SPI-compatible serial interface for

writing to the 24bit shift register. CLK, DATA, and LE control the data transfer.

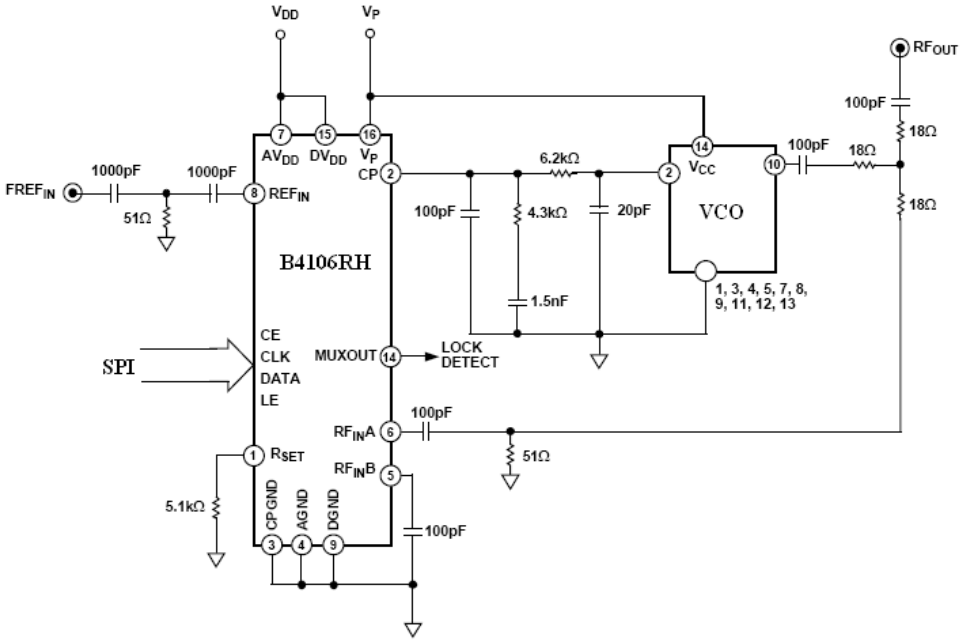


Figure 8-1 typical application circuit diagram

9. Package Specifications

The specifications of FP16 package are shown in figure 9-1.

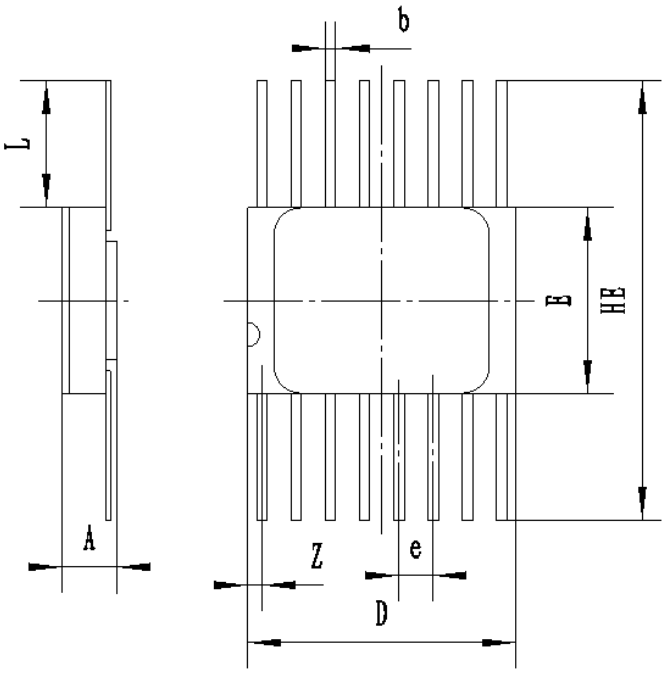


Figure 9-1 FP16 package specifications

Table 9-1 size symbol list

Size symbol	Value （unit：mm）		
	min	typical	max
A	1.77	—	2.56
b	0.25	—	0.54
c	0.07	—	0.20
e	—	1.27	—
Z	20.00	—	25.00
D	—	—	1.27
E	9.28	—	10.64
HE	6.36	—	7.46
L	6.27	—	7.99

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