5GHz Radiation hardened wideband integer-N frequency synthesizer

Datasheet

Part Number: BM7101MQRH



Ver 2.0



Page of Revise Control

Version No.	Publish Time	Revised Chapter	Revise Introduction	Note
1100		Chapter		
1.0	2017/04/05		Initial Revision	
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TABLE OF CONTENTS

1.	Features1
2.	General Description
3.	Function Block Diagram
4.	Packages and Pin Function Descriptions
5.	Detailed Description
	5.1 Function Description
	5.2 Storage Condition
	5.3 Absolute Maximum Ratings9
	5.4 Recommended Operation Conditions9
6.	Specifications9
7.	Notice
8.	Typical Application12
9.	Package Specifications



1. Features

Scrubbing features

- Programmable dual-modulus prescaler: 8/9, 16/17, 32/33, 64/65
- Programmable antibacklash pulse width
- Hardwired programmable
- Digital lock detect
- Hardware power-down mode
- Without internal register
- Package: CQFP48
- Electrical characteristics
 - 3.0V to 3.6V supply voltage

- RF input frequency range : 0.5GHz ~ 5GHz
- Reference input frequency range : 10MHz ~ 200MHz
- Reliability features
 - Operating temperature : -55℃ ~ +125℃
 - ESD (human body model) : 2000V
 - Total ionizing dose : ≥ 100Krad(Si)
 - Single event latch-up threshold : $\geq 75 \text{MeV} \cdot \text{cm}^2/\text{mg}$

2. General Description

The BM7101MQRH frequency synthesizer can be used to implement local oscillators in the up-conversion and down-conversion sections of wireless receivers and transmitters. It consists of a low noise, digital phase frequency detector (PFD), a precision charge pump, a programmable reference divider, programmable A counter and B counter, and a dual-modulus prescaler (P/P + 1). The A (4-bit) counter and B (10-bit) counter, in conjunction with the dual-modulus prescaler (P/P + 1), implement an N divider (N = BP + A). In addition, the 6-bit reference counter (R Counter) allows selectable REF_{IN} frequencies at the PFD input. A complete phase-locked loop (PLL) can be implemented if the synthesizer is used with an external loop filter and voltage controlled oscillator (VCO). It's very high bandwidth means that frequency doublers can be eliminated in many high frequency systems, simplifying system architecture and reducing cost.

3. Function Block Diagram



BM7101MQRH function block diagram is shown in figure 3-1.

Figure 3-1 BM7101MQRH function block digram

4. Packages and Pin Function Descriptions

The provided package is: CQFP48.

BM7101MQRH CQFP48 pin configuration is shown in 4-1, in top view the pin P1 is in the bottom of the left side, the pins are arranged in anticlockwise order.



Figure 4-1 CQFP48 pin configuration



究所 Institute		
nction Des	scriptio	ons
Terminal	Pin	Function

Talble 4-1 BM7101MQRH Pin Function Descriptions

No. Symbol Type No. Symbol Type International Constraints 1 CPGND GND Charge pump Ground 25 M9 I B Counter Bit9 2 AGND GND Analog Ground 26 M8 1 B Counter Bit9 3 Rser IO Biss for charge pump 27 M7 I B Counter Bit9 4 MUXOUT_MI I MUXOUTCourtol 28 M6 I B Counter Bit9 5 MUXOUT_MI I MUXOUT Courtol 29 M5 I B Counter Bit9 6 MUXOUT_MI I MUXOUT Courtol 20 M5 I B Counter Bit9 7 PD1 I MUXOUT Courtol 30 M4 I B Counter Bit9 8 NCC I MUXOUT Courtol 30 M4 I B Counter Bit9 9 RFibN I Forecaler 33 M1 I B Counter Bit9 10 RFibN I Input to the RF Prescaler 33 M1 <td< th=""><th>Pin</th><th colspan="2">Terminal Pin Function</th><th>Pin</th><th>Terminal</th><th>Pin</th><th>Function</th></td<>	Pin	Terminal Pin Function		Pin	Terminal	Pin	Function	
1 CPGND GND Charge pump Ground 25 M9 1 B Counter Bid 2 AGND GND Analog Ground 26 M8 1 B Counter Bid 3 Rsrr IO Bias for charge pump 27 AM7 1 B Counter Bid 4 MUXOUT_M1 10 MUXOUTCourol 28 M64 1 B Counter Bid 5 MUXOUT_M1 1 MUXOUTCourol 28 M64 1 B Counter Bid 6 MUXOUT_M1 1 MUXOUTCourol 20 M4 1 B Counter Bid 7 PD1 1 MUXOUT Courol 31 MA4 1 B Counter Bid 8 MUXOUT_M1 1 MUXOUT Courol 32 MA4 1 B Counter Bid 9 MEF_M8 I MUXOUT Courol 32 MA4 I B Counter Bid 9 MEF_M8 I Imput to the RF 33 MUT I B Counter Bid </td <td>No.</td> <td>Symbol</td> <td>Туре</td> <td>i unction</td> <td>No.</td> <td>Symbol</td> <td>Туре</td> <td>i unction</td>	No.	Symbol	Туре	i unction	No.	Symbol	Туре	i unction
1 AGND GND Analog Ground 26 M8 I B Counter Bids 3 RSTT ID Bias for charge pump 2 AM7 II B Counter Bids 4 MUXOUT,MI I MUXOUTCOURD 28 AM6 I B Counter Bids 5 MUXOUT,MI I MUXOUTCOURD 20 AM6 I B Counter Bids 6 MUXOUT,MI I MUXOUTCOURD 20 AM6 I B Counter Bids 7 PD1 I MUXOUTCOURD 30 AM6 I B Counter Bids 8 MUXO I MUXOUTCOURD 30 IAM8 I B Counter Bids 8 MUXO I MUXOUTCOURD 30 IAM8 I B Counter Bids 9 PRF I Complementary A AM1 I B Counter Bids 9 RF _{IN} A I Input to the RF A A AM1 I B Counter Bids 10 RF _{IN} A I Input to the RF A A A A A 11 Prescaler Input to the RF A A A A A A	1	CPGND	GND	Charge pump Ground	25	M9	Ι	B Counter Bit9
3 Rsrr I/O Bias for charge pupp 2/I MAN II Be couter Bid 4 MUXOUT,M I MUXOUTCOURO 28 M64 I B Couter Bid 5 MUXOUT,M2 I MUXOUTCOURO 20 M04 I B Couter Bid 6 MUXOUT,M2 I MUXOUTCOURO 20 M04 I B Couter Bid 7 PD1 I MUXOUTCOURO 20 M04 I B Couter Bid 7 PD1 I MUXOUTCOURO 20 M04 I B Couter Bid 8 NCC I Power Down 31 MAG I B Couter Bid 7 PD1 I Complements A A I B Couter Bid 9 RFisB I Input to the RF A A A A 10 RFisA I Input to the RF A A A A 11 Prescaler B A A A A A 11 Prescaler B A A A A A 12 Prescaler B A A A A A<	2	AGND	GND	Analog Ground	26	M8	Ι	B Counter Bit8
14 MUXOUT,M I MUXOUT Control 28 M6 I B Counter Bid 5 MUXOUT,M I MUXOUT Control 30 M4 I B Counter Bid 6 MUXOUT,M I MUXOUT Control 30 M4 I B Counter Bid 7 PDI I Power Down 31 MA I B Counter Bid 8 NC I Power Down 32 MA I B Counter Bid 8 NC I Power Down 32 MA I B Counter Bid 9 PRP. I Complementary 32 MA I B Counter Bid 9 PRFmR I Input to the RF 33 PA Pa Paconter Bid 10 PRFmA I Input to the RF 34 PMO I B Counter Bid 11 Prescaler 34 Prescaler 34 PMO I B Counter Bid 11 Prescaler Value 34 PO P Putolytopy Putolytopy 13 Prescaler Value 34 POL P Putolytopy Putolytopy 14 PA P Paconter Sid	3	R _{SET}	I/O	Bias for charge pump	27	M7	Ι	B Counter Bit7
MUXOUT,MU I MUXOUTCOMID 20 MMS I BCOMERBIS MUXOUT_MU I MUXOUTCOMID 30 MMA I BCOMERBIA P PDI I Power Down 31 MA I BCOMERBIA NC I Power Down 32 MA I BCOMERBIA MUXOUT,MU I Power Down 32 MA I BCOMERBIA MUXOUT,MU I Power Down 32 MA I BCOMERBIA MUXOUT,MU I Power Down 32 MA I BCOMERBIA Muxout,	4	MUXOUT_M1	Ι	MUXOUT Control	28	M6	Ι	B Counter Bit6
MUXOUT_M I MUXOUT Control 30 M44 I B Counter Bid P PDI I Power Down 31 M33 II B Counter Bid 8 NC I NC 32 M33 II B Counter Bid 9 PREMB I Complementary Input othe RF 33 M1 I B Counter Bid 9 PREMB I Input othe RF 33 M1 I B Counter Bid 10 PREMB I Input othe RF 34 M00 I B Counter Bid 11 Prescaler Prescaler Prescaler P Muxout Muxout Muxout 11 Prescaler P Prescaler P Muxout Muxout Muxout 11 Prescaler P P Muxout P Muxout Muxout 11 Prescaler P P Muxout P Muxout Muxout 11 Prescaler P P Muxout P Muxout Muxout 11 Prescaler P P P P P P 11 Prescaler P P P P	5	MUXOUT_M2	Ι	MUXOUT Control	29	M5	Ι	B Counter Bit5
7 PD1 1 Power Down1 31 M3 1 B Counter Bit3 8 NC I NC 32 M2 I B Counter Bit3 9 RFINB I Complementary Input to the RF 33 AM1 I I B Counter Bit1 10 RFINA I Input to the RF 34 MUXOUT I B Counter Bit1 11 pre_sel1 I Input to the RF 35 MUXOUT O Muxtiplexer Output 11 pre_sel2 I Prescaler Value Control 35 MUXOUT O Muxtiplexer Output 12 pre_sel2 I Prescaler Value Control 36 DVpob Vpb Muxtiplexer Output 13 ANpob I Prescaler Value Control 36 DVpob Vpb Muxtiplexer Output 14 F3 I Prescaler Value Control 36 DVpob Vpb Muxtiplexer Output 13 ANpob Vpb I Prescaler Value Control 37 PD_DN Qp PEDOutput 14 F3 I COThree-State 38 PD_UP I RCounter Bit0 15 F2 I Phase Detector Polarity C	6	MUXOUT_M3	Ι	MUXOUT Control	30	M4	Ι	B Counter Bit4
8 NC I NC 32 M2 I B Counter Bi2 9 RFinB I Complementary Input to the RF 33 MI I B Counter Bi1 10 RFinB I Input to the RF Prescaler 34 M0 I B Counter Bi1 11 Prescaler 34 M0 I B Counter Bi1 11 pre_sel1 I Prescaler Value Control 34 MUXOUT O Mutiplexer Output 12 pre_sel2 I Prescaler Value Control 36 DV _{DD} Q Mutiplexer Output 13 AV _{DD} I Prescaler Value Control 36 DV _{DD} Q Mutiplexer Output 14 AV _{DD} I Analog supply voltage 37 PD_DN Q PfeD Output 15 F2 I Phase Detector Polarity Control 38 PD_LON I RCounter Bi1 16 DGND GN I Reference Input 40 R1 I RCounter Bi1 17 REFin I ReferenceInput	7	PD1	Ι	Power Down1	31	M3	Ι	B Counter Bit3
9 RF _{IN} B I Complementary Input to the RF Prescaler 33 M1 I B Counter Bitl 10 RF _{IN} A I Input to the RF Prescaler 34 M0 I B Counter Bitl 11 Prescaler 1 Input to the RF Prescaler 34 M0 I B Counter Bitl 11 Prescaler 34 M0 I B Counter Bitl 11 Prescaler Value Control 36 MUXOUT O Muxtiplexer Output 12 Prescaler 1 Prescaler Value Control 36 DV _{DD} V _{DD} Amalog supply Output 37 DV _{DD} V _{DD} Amalog supply Output 37 PD_DN Q PFEDOutput 13 AV _{DD} V Amalog supply Voltage 37 PD_DN Q PFEDOutput 14 F3 I CAPTore-State 38 PD_DN Q PFEDOutput 15 F2 I Phase Detector Polarity Control 38 PD_UN I R Counter Bitl 16 DGND GND I Reference Input 40 R1 I R Counter Bitl 17 REF_IN I ReferenceInput 41 R2 R3 <t< td=""><td>8</td><td>NC</td><td>Ι</td><td>NC</td><td>32</td><td>M2</td><td>Ι</td><td>B Counter Bit2</td></t<>	8	NC	Ι	NC	32	M2	Ι	B Counter Bit2
10 RF _{IN} A 1 Input to the RF Prescaler 2 MO I B Counter Bid 11 Prescaler Prescaler Value Courtor 25 MUXOUT 0 Muxiplexer Output 12 Prescaler Prescaler Value Courtor 26 DVpob 0 Muxiplexer Output 13 Prescaler Prescaler Value Courtor 26 DVpob Vpob Output Output 14 Prescaler Prescaler Value Courtor 26 DVpob Vpob Output Output 15 AVpob Pt Analog supply voltage 27 PD_DN O PEDOutput 16 AVpob Pt Prescaler Value voltage 37 PD_DN O PEDOutput 15 F2 I Phase Detector Polarity Courtor 38 RR0 I RCounter Bid 16 DGND I Reference Input 40 RA I RCounter Bid 17 RABP1 I Pigial Lock Detector Output IA	9	RF _{IN} B	Ι	Complementary Input to the RF Prescaler	33	M1	Ι	B Counter Bit1
11 pre_sel1 I Prescaler Value Control 34 PMUXOUT 60 PMUXiplexer Output 12 pre_sel2 I Prescaler Value Control 34 DVpD VpD Page 13 pre_sel2 I Prescaler Value Control 34 DVpD VpD Page 14 Prescaler VpD Prescaler Value Control 37 PD_DN VpD Page 14 PAVpD VpD VpD Prescaler Value Control 37 PD_DN Q PFDOutput 15 PAVpD VpD VpD Prescaler Value Control 37 PD_DN Q PFDOutput 16 F3 I POPase Detector Polarity Control 38 PD_UP I RCounter Bit0 16 DGND GND IDigital Ground 40 R1 I RCounter Bit1 17 REF_IN I Reference Input 41 R2 I RCounter Bit1 18 LD_OUT I Igital Lock Detector Output IR IR IRCounter Bit3 19 PABPI I Igital Lock Detector Output R3 RAN IR IR 19 ABPI I Igital Lock Det	10	RF _{IN} A	Ι	Input to the RF Prescaler	34	M0	Ι	B Counter Bit0
12 ppe_sel2 I Prescaler Value Control 36 DVpp Vpp Pdgala supply volage 13 AVpp V_{DD} V_{DD} Analog supply volage 37 PD_DN Q PFD Output 14 F3 I CPThree-State 38 PD_UP O PFD Output 14 F3 I CPThree-State 38 PD_UP O PFD Output 15 F2 I Phase Detector Polarity Control 39 R0 I RCounter Bit0 16 DGND GND I Pface Detector Polarity Control 39 R0 I RCounter Bit0 16 DGND GND I Reference Input 40 R1 I RCounter Bit3 17 REF _{IN} I Reference Input 41 R2 I RCounter Bit3 18 LD_OUT O Digital Lock Detector Output 42 R3 I RCounter Bit3 19 ABP1 I ANTIBACKLASH Output 42 R3 I PFD Ground 20 A3 I ACounter Bit3 OHN PGN PGN PGN	11	pre_sel1	Ι	Prescaler Value Control	35	MUXOUT	0	Muxtiplexer Output
13 AVDD VDD Analog supply voltage 37 PD_DN O PFD Duput 14 F3 I CP Three-State 38 PD_UP O PFD Output 15 F2 I Phase Detector Polarity Control 39 RO I R Counter BitO 16 DGND GND GND Digital Ground 40 R1 I R Counter BitO 17 REF _{IN} I Reference Input 41 R2 I R Counter BitO 18 LD_OUT O Digital Lock Detect Output 42 R3 I R Counter Bit3 19 ABP1 I ANTIBACKLASH Pulse Width Control 43 DGND_PFD GND PFD Ground 20 A3 I ACounter Bit3 44 DVp_PFD Vp_D PFD Ground	12	pre_sel2	Ι	Prescaler Value Control	36	DV_DD	V _{DD}	Digital supply voltage
14F3ICP Three-State38PD_UPOPFD Output15F2IPhase Detector Polarity Control39R0IR Counter BitO16DGNDGNDDigital Ground40R1IR Counter BitO17REF1NIReference Input41R2IR Counter BitO18LD_OUTODigital Lock Detect Output42R3IR Counter BitO19ABP1IANTIBACKLASH Plas Width Control43DON_PFDRNPFD Ground20A3IA Counter BitO44DVp_PFDVpPFD supply voltage	13	AV _{DD}	V _{DD}	Analog supply voltage	37	PD_DN	0	PFD Output
15F2IPhase Detector Polarity Control39R0IR Counter BitO16DGNDGNDDigital Ground40R1IR Counter Bit117REFINIReference Input41R2IR Counter Bit218LD_OUTODigital Lock Detect Output42R3IR Counter Bit319ABP1IANTIBACKLASH Pulse Width Control43DVp_PFDGNDPFD Ground20A3IA Counter Bit344DVp_D_FFDVp_DPFD supply voltage	14	F3	Ι	CP Three-State	38	PD_UP	0	PFD Output
16DGNDGNDDigital Ground40R1IR Counter Bit117REF1NIReference Input41R2IR Counter Bit218 LD_OUT ODigital Lock Detect Output42R3IR Counter Bit319ABP1IANTIBACKLASH Pulse Width Control43DGND_PFDGNDPFD Ground20A3IA Counter Bit344DV_D_PFDV_DPFD supply voltage	15	F2	Ι	Phase Detector Polarity Control	39	R0	Ι	R Counter Bit0
17REF1NIReference Input41R2IR Counter Bit218 LD_OUT ODigital Lock Detect Output42R3IR Counter Bit319ABP1IANTIBACKLASH Pulse Width Control43DGND_PFDGNDPFD Ground20A3IA Counter Bit344DV_DD_PFDV_DDPFD supply voltage	16	DGND	GND	Digital Ground	40	R1	Ι	R Counter Bit1
18 LD_OUT ODigital Lock Detect Output42R3IR Counter Bit319 $ABP1$ I $ANTIBACKLASH$ Pulse Width Control43 $DGND_PFD$ GND $PFD Ground$ 20A3IA Counter Bit344 DV_{DD}_PFD V_{DD} $PFD supply voltage$	17	$\operatorname{REF}_{\operatorname{IN}}$	Ι	Reference Input	41	R2	Ι	R Counter Bit2
19ABP1A HANTIBACKLASH Pulse Width Control43DGND_PFDGNDPFD Ground20A3IA Counter Bit344DV_DD_PFDV_DDPFD supply voltage	18	LD_OUT	0	Digital Lock Detect Output	42	R3	Ι	R Counter Bit3
20 A3 I A Counter Bit3 44 DV _{DD} _PFD V _{DD} PFD supply voltage	19	ABP1	Ι	ANTIBACKLASH Pulse Width Control	43	DGND_PFD	GND	PFD Ground
	20	A3	Ι	A Counter Bit3	44	DV _{DD} _PFD	V _{DD}	PFD supply voltage

Pin	Terminal	Pin	Function	Pin	Terminal	Pin	Eunction
No.	Symbol	Туре	Function	No.	Symbol	Туре	Function
21	A2	Ι	A Counter Bit2	45	R4	Ι	R Counter Bit4
22	A1	Ι	A Counter Bit1	46	R5	Ι	R Counter Bit5
23	A0	Ι	A Counter Bit0	47	СР	0	Charge pump output
24	CF	CE	Chin Enable	19	VP	V	Charge pump power
24	CE			40	۷I	▼ DD	supply

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5. Detailed Description

5.1 Function Description

The main functions of BM7101MQRH are as follows:

1) Prescaler

T The dual-modulus prescaler (P/P + 1), along with the A counter and B counter, enables the large division ratio, N, to be realized (N = BP + A). The dual-modulus prescaler, operating at CML levels, takes the clock from the RF input stage and divides it down to a manageable frequency for the CMOS A counter and B counter. The prescaler is programmable. It can be set to 8/9, 16/17, 32/33, or 64/65. It is based on a synchronous 4/5 core. There is a minimum divide ratio possible for fully contiguous output frequencies. This minimum is determined by P, the prescaler value, and is given by (P2 – P).

pre_sel2 and pre_sel1 set the prescaler values. The prescaler value should be chosen so that the prescaler output frequency is always less than or equal to 325 MHz. Therefore, with an RF frequency of 4 GHz, a prescaler value of 16/17 is valid, but a value of 8/9 is not valid.

pre_sel2	pre_sel1	Pescaler Value
0	0	8/9
0	1	16/17
1	0	32/33
1	1	64/65

Talble 5-1 Pescaler Value

2) Power Down

PD1 provides power-down modes. It is enabled by the CE pin.

When the CE pin is low, the device is immediately disabled regardless of the states of PD1.

CE	PD1	MODE
0	Х	ASYNCHRONOUS POWER-DOWN
1	0	NORMAL OPERATION
1	1	SYNCHRONOUS POWER-DOWN

Note: When the PLL circuit is operating abnormally, the PLL circuit can be reset through the CE pin without having to return on the power.

3) MUXOUT Control

The on-chip multiplexer is controlled by MUXOUT_M3, MUXOUT_M2, and MUXOUT_M1. The table shows the truth table. The N-channel, open-drain, analog lock detect should be operated with an external pull-up resistor of 10 k Ω nominal. When lock is detected, this output is high with narrow, low-going pulses.

Caution: It is necessary to declare that, the MUXOUT output is used to test whether the circuit inside the chip is working correctly or not, and this port should be set to "Three-State Output" (MUXOUT_M3=0, MUXOUT_M2=0, MUXOUT_M1=0) to ensure the correct work of the frequency synthesizer. Otherwise, when MUXOUT "R Divider Output" (MUXOUT M3=1, MUXOUT M2=0, is set to MUXOUT_M1=0), or "N Divider Output" (MUXOUT_M3=0, MUXOUT_M2=1, MUXOUT_M1=0), the phase noise at the radio frequency output port of frequency synthesizer may deteriorate and the frequency synthesizer is likely to fail to lock at a high output frequency.

MUXOUT_M3	MUXOUT_M2	MUXOUT_M1	OUTPUT
0	0	0	Three-State Output
0	0	1	Reserved
0	1	0	N Divider Output
0	1	1	DV _{DD}
1	0	0	R Divider Output
1	0	1	N-CHANNEL Open-Drain Lock Detect
1	1	0	Reserved
1	1	1	DGND

Talble 5-3 MUXOUT

4) A counter and B counter

The A counter and B counter, in conjunction with the dual-modulus prescaler,



make it possible to generate output frequencies that are spaced only by the reference frequency divided by R. The equation for the VCO frequency is

 $f_{VCO} = [(P \times B) + A] \times f_{REFIN}/R$

where:

 $f_{\rm VCO}$ is the output frequency of the external voltage controlled oscillator (VCO).

P is the preset modulus of the dual-modulus prescaler (8/9, 16/17, etc.).

B is the preset divide ratio of the binary 9-bit counter (3 to 1023).

A is the preset divide ratio of the binary 4-bit swallow counter (0 to 15).

R is the preset divide ratio of the binary 5-bitRcounter (1 to 63).

 f_{REFIN} is the external reference frequency oscillator.

A3	A2	A1	A0	A Counter Divider Ratio
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
1	1	1	0	14
1	1	1	1	15

Talble 5-4 A Counter

M9	M8	M7		M2	M1	M0	B Counter Divider Ratio
0	0	0		0	0	0	Not Allowed
0	0	0	•••	0	0	1	Not Allowed
0	0	0	•••	0	1	0	Not Allowed
0	0	0		0	1	1	3
1	1	1		1	0	0	1020
1	1	1		1	0	1	1021
1	1	1		1	1	0	1022
1	1	1		1	1	1	1023

5) R counter

The 5-bit R counter allows the input reference frequency to be divided down to

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produce the reference clock to the phase frequency detector (PFD). Division ratios from 1 to 63 are allowed.

R5	R4	R3	R2	R1	R0	R Counter Divider Ratio
0	0	0	0	0	1	1
0	0	0	0	1	0	2
0	0	0	0	1	1	3
1	1	1	1	1	0	62
1	1	1	1	1	1	63

Talble 5-6 R Counter

6) Phase Detector Polarity

This bit sets the phase detector polarity bit. When using a passive loop filter or non-inverting active loop filter, this must be set to "1", If using an active filter with an inverting characteristic, it must be set to "0".

Talble 5-7 Phase Detector Polarity

F2	Phase Detetor Polarity
0	Negative
1	Positive

7) Anti-backlash Pulse Width

The PFD includes a programmable delay element that controls the width of the anti-backlash pulse. This pulse ensures that there is no dead zone in the PFD transfer function and minimizes phase noise and reference spurs. ABP1 control the width of the pulse.

Talble 5-8 Anti-backlash Pulse Width

ABP1	Anti-backlash Pulse Width			
0	2.9ns			
1	1.3ns			

8) Charge Pump Output

F3 controls the CP output pin. With the bit set high, the CP output is put into three-state. With the bit set low, the CP output is enabled.

Talble 5-9 Charge Pump Output

F3	Charge Pump Output			
0	Normal			
1	Three-State			



9) Bias for charge pump

Connecting a resistor between this pin and GND sets the charge pump output current. The nominal voltage bias at the R_{SET} pin is 0.65 V. The relationship between I_{CP} and R_{SET} is : when R_{SET} =5.1K Ω , I_{CP} =3.0mA.

10) RF Input

The RF input stage is shown in Figure 7. It is followed by a 2-stage limiting amplifier to generate the CML clock levels needed for the prescaler.



Figure 5-1 RF input stage

11) PFD Output

The phase detector is triggered by rising edges from the A/B counter(fp) and the reference counter(fc). It has two outputs namely PD_UP and PD_DN. PD_UP and PD_DN are designed to drive an active loop filter which controls the VCO tune voltage.

12) Lock Detect

When the PLL is in lock, the digital lock detect LD_OUT is open-drain output, otherwise LD_OUT is a logic low("0"). When five consecutive cycles of less than 15ns pulse width are detected, the LD_OUT is set to high. It stays set high until a phase error of greater than 25ns is detected on any subsequent PFD cycle. When pulse width of LD_in is bigger than 15ns and smaller than 25ns, LD_OUT keeps lock state, and the lock detect circuit is disabled to reduce power consumption.

5.2 Storage Condition

Packaged product should be stored in the ventilate warehouse with ambient temperature $10^{\circ}C \sim 30^{\circ}C$ and relative humidity less than 70%. There should be no acid, alkali or other radiant gas in the environment.



5.3 Absolute Maximum Ratings

- a) Supply voltage (AV_{DD}, DV_{DD} , DV_{DD} , PFD, V_P) : -0.3V ~ 3.9V
- b) Voltage on any input (V_I) : -0.3 V ~ V_{DD}+0.3V
- c) Operation temperature range (T_A) : -55 °C ~125 °C
- d) Storage temperature range (T_{stg}) : -65 °C ~ 150 °C
- e) Maximum Junction Temperature (T_J) : 150 °C
- f) Thermal resistance $(R_{th(J-C)}) : 5^{\circ}C/W$
- g) Lead Temperature 10s (T_H) : 260 °C

5.4 Recommended Operation Conditions

- a) Supply voltage (AV_{DD}, DV_{DD} , DV_{DD} , PFD, V_P) : 3.0V ~ 3.6V
- b) Operation temperature range(T_A) : -55 °C ~ 125 °C

6. Specifications

All electrical characteristics are shown in table 6-1. $AV_{DD} = DV_{DD} = DV_{DD}$ _PFD = $V_P = 3.0V$ to 3.6V, AGND = DGND = DGND_PFD = CPGND = 0 V, dBm referred to 50 Ω , $T_A = -55$ °C to 125 °C, unless otherwise noted.

 Table 6-1 BM7101MQRH electrical characteristics

Parameter	min	typ	max	Unit	Test conditions/comments		
RF CHARACTERISTICS							
RF Input Frequency(RF _{IN}) ¹	0.5	-	5.0	GHz	For lower frequencies, ensure		
RF Input Sensitivity	-5	-	5	dBm	siew rate $(SK) > 320 \sqrt{\mu S}$		
REF _{IN} CHARACTERISTIC	REF _{IN} CHARACTERISTICS						
REF _{IN} Input Frequency	10	-	200	MHz	For f<20MHz, ensure SR > $50V/\mu$ S,		
REF _{IN} Input Sensitivity ²	0.8	-	V _{DD}	Vp-p	Biased at VDD/2.		
REF _{IN} Input Current	-100	-	100	uA			
PHASE DETECTOR							
Phase Detector Frequency	-	-	20	MHz			
PHASE DETECTOR OUTPUT							
PD_DN	-	-	20	MHz			

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PD_UP	-	-	20	MHz		
LD_OUT	0.4	-	DV _{DD} -0.4	V		
CHARGE PUMP						
I _{CP} Sink/Source Value	-	2.5	-	mA	RSET=5.1KΩ	
LOGIC INPUTS	LOGIC INPUTS					
V _{IH} , Input High Voltage	2.0	-	-	V		
V _{IL} , Input Low Voltage	-	-	0.7	V		
I _{INH} , I _{INL} , Input Current	-100	-	100	uA	DV _{DD} =3.6V	
LOGIC OUTPUTS	L	ı	L	1		
V _{OH} , Output High Voltage	DV _{DD} -0.4	-	-	v	CMOS output, I _{OH} = -100uA	
V _{OL} , Output Low Voltage	-	-	0.4	V	I _{OL} = 500uA	
POWER SUPPLIES						
AV _{DD} =DV _{DD} _PFD=DV _{DD}	3.0	-	3.6	V		
VP	AV _{DD}	-	3.6	V		
I _{DD}		15		mA	TA=25 °C, AV _{DD} =DV _{DD} _PFD=DV _{DD} =V _P =3.3V P=32, RF _{IN} =5.0GHz	
NOISE CHARACTERISTI	CS				I	
Normalized Phase Noise Floor ³	-	-219	-	dBc/Hz		
Dhaan Maiaa	-	-93	-	dBc/Hz	@10KHz offset,f _{PFD} =10MHz , @4.95GHz	
Phase Noise	-	-82	-	dBc/Hz	@10KHz offse, f _{PFD} =1MHz , @4.95GHz	
S	-	-67	-	dBc	@1MHz offse,f _{PFD} =1MHz , @4.95GHz	
Spur	-	-72	-	dBc	@2MHz offse,f _{PFD} =1MHz , @4.95GHz	

Note1. If the minimum reference frequency and the RF input frequency of BM7101MQRH need to be less than 20MHz and 500MHz respectively, adding an additional clock buffer is necessary.

Note2. AC coupling ensures $V_{DD}/2$ bias.

Note3. The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20log N (where N = BP + A) and $10\log f_{PFD}$. PN_{SYNTH} = PN_{TOT} -10log f_{PFD} -20log N.

7. Notice

1) The RF and REF input signals need sufficient slew rate at different operating frequencies to ensure the dividers work correctly (SR $\ge 2 \times \pi \times f \times V_P$, f is the input frequency, V_P is the input amplitude). For example, when the input frequency f is 500MHz and the input amplitude V_P is 0dBm, the slew rate SR needs to be larger than 942V/us.

In addition, the RF input stage is differential input. If a single input is used in application, unused input must be grounded with a capacitor, and the value must be the same as the DC-blocking capacitor at the used input.

2) The off-chip LPF directly affects the phase noise and lock time of the frequency synthesizer. In the case of low noise applications, the passive LPF is used to convert the charge pump output current into a control voltage usually. In the circuit design, it is recommended to use the third-order LPF to improve the suppression of spurious signals.

3) The MUXOUT port is only used to detect the internal signal state. When turned on, it may deteriorate the noise performance of the frequency synthesizer, and even cause the PLL to be loss of lock. When the PLL is working properly, the MUXOUT port should be set to the three-state output.

4) In the space environment, the single-event effect may cause functional interruptions of the device and cannot be automatically recovered. When the lock signal (LD_OUT) is low, the device needs to be reset through the CE port and refresh the register.

5) In application, the main characteristic parameters of the device, such as the PFD frequency, CP current and etc. should be designed and optimized with the characteristic parameters of off-chip VCO and LPF to ensure the frequency synthesizers work properly.

6) The bandwidth of off-chip LPF is between one tenth and one fifteen of the PFD frequency. When PFD frequency is too high, the bandwidth is out of this range that may cause the PLL to be loss of lock. The PFD frequency should be designed properly in application.

7) The RF input port and off-chip VCO output port should be impedance matched and the connection of these ports should be designed as short as possible.

8) The ripple of the power supply voltage will affect the working state of the device. When the voltage ripple is too large, the device may be loss of lock. Therefore,



it is recommended to use a low dropout regulator (LDO) as the power supply.

9) The power supply of the device, such as analog power supply (AV_{DD}) , digital power supply (DV_{DD}) , PFD power supply (DV_{DD}_PFD) and CP power supply (V_P) , should have good decoupling. Decoupling capacitors should be placed as close as possible to those pins.

8. Typical Application

The circuit diagram of BM7101MQRH typical application is shown in figure 8-1. The reference input signal is applied to the circuit at FREF_{IN} with a TCXO or another low noise frequency source. The third-order LPF output (The values of R and C are typical values in figure 8-1. That need to be optimized according to the condition of the PLL loop.) drives the VCO, which in turn is fed back to the RF input of the PLL synthesizer and also drives the RF output terminal. The MUXOUT pin can be programmed to monitor various internal signals in the synthesizer.



Figure 8-1 typical application circuit diagram

9. Package Specifications

The specifications of CQFP48 package are shown in figure7-1.



Figure 7-1 CQFP48 package specifications

Cize symbol	Value (unit: mm)				
Size symbol	min	typical	max		
А	2.1		2.7		
A1	1.98		2.3		
b	0.15		0.25		
с		0.15			
e		0.5			
Z		1.15			
D/E	7.6	7.8	8.0		
D1/E1	30.0		30.6		
L		7.75			

Table 7-1 size symbol list

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