Ver 1.2

16-Bit 1GSPS Digital to Analog Converter

Datasheet

Part Number：B9122RH

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Page of Revise Control

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1.0	2017.1	-	-	
1.1	2018.3	-	Changed the template	
1.2	2018.9	Page 54	Add the EPAD Dimension	

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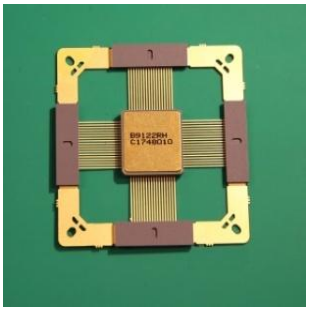
1. Features



- Flexible LVDS interface allows word, byte, or nibble load
- Analog output: adjustable 9 mA to 30 mA, R_L = 25 Ω to 50 Ω
- Integrated 2×/4×/8× interpolator/complex modulator allows carrier placement anywhere in the DAC bandwidth
- Gain, dc offset, and phase adjustment for sideband suppression
- Multiple chip synchronization interfaces
- High performance, low noise PLL clock multiplier
- Digital inverse sinc filter
- Low power(full operating conditions): 1.5 W at 1 GSPS
- 72-lead, CQFP Package
- Total Ionizing Dose ≥ 100 Krad(Si)
- SEL threshold ≥ 75 MeV ɕcm^2/mg

2. Applications

Wireless infrastructure

W-CDMA, CDMA2000, TD-SCDMA, WiMAX, GSM, LTE Digital high or low IF synthesis

Transmit diversity

Wideband communications: LMDS/MMDS, point-to-point

3. General Description

The B9122RH is a dual, 16-bit, high dynamic range digital-to- analog converter (DAC) that provides a sample rate of 1000 MSPS, permitting multicarrier generation up to the Nyquist frequency. The B9122RH includes features optimized for direct conversion transmit applications, including complex digital modulation, and gain and offset compensation. The DAC outputs are optimized to interface seamlessly with analog quadrature modulators, such as the ADL537x F-MOD series from Analog Devices, Inc. A 4-wire serial port interface provides for programming/readback of many internal parameters. Full-scale output current can be programmed over a range of 9 mA to 30 mA. The B9122RH comes in a 72-lead CQFP package.

Product highlights

1. Ultralow noise and intermodulation distortion (IMD) enable high quality synthesis of wideband signals from baseband to high intermediate frequencies (IF).
2. Proprietary DAC output switching technique enhances dynamic performance.
3. Current outputs are easily configured for various single-ended or differential circuit topologies.
4. Flexible LVDS digital interface allows the standard 32-wire bus to be reduced to one-half or one-quarter of the width.

4. Functional block

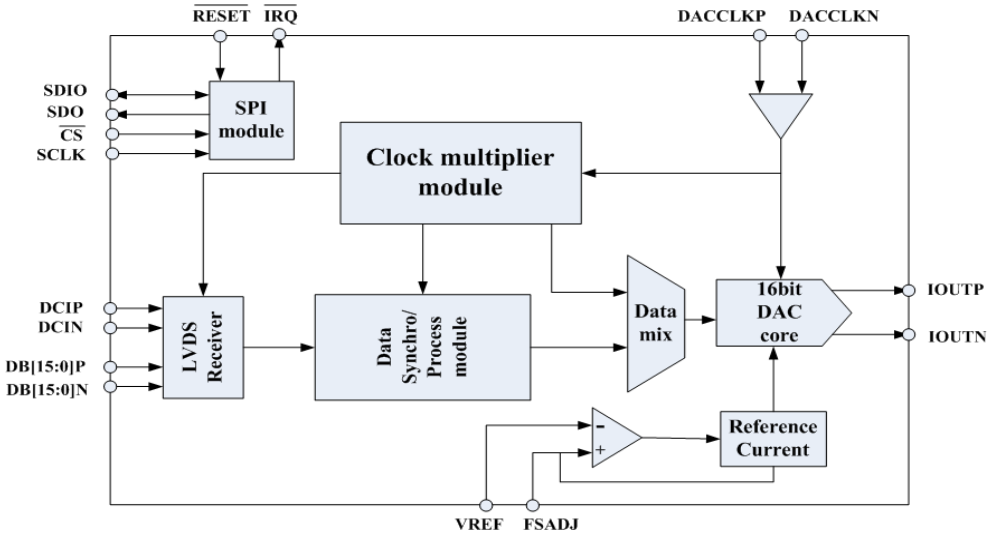


Figure 4-1 Functional block diagram

5. Specifications

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, IOVDD = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{FS} = 20 mA, maximum sample rate, unless otherwise noted.

Table 5-1 Electrical Specifications

Parameter	Symbol	Test Condition (V_{IOVDD}=V_{AVDD33} = 3.3 V、V_{CVDD18} = V_{DVDD18} =1.8 V、I_{OUTFS} = 20 mA、-55℃ ≤ T_A≤ 125℃)	Min	Max	Unit
Resolution	*RES*	—	16	—	Bits
DNL	E_{DL}	—	-3.5	+3.5	LSB
INL	E_L	—	-5.5	+5.5	LSB

Parameter	Symbol	Test Condition (V_{IOVDD}=V_{AVDD33} = 3.3 V、V_{CVDD18} = V_{DVDD18} =1.8 V、I_{OUTFS} = 20 mA、-55℃ ≤ T_A≤ 125℃)		Min	Max	Unit
Gain Error	E_G	—		-5.5	+5.5	%FSR
Offset Error	E_O	—		-2	+2	%FSR
Internal Reference Voltage	V_{REF}	—		1.18	1.32	V
Minimum Full-Scale Output Current	I_{FS_min}	—		—	9	mA
Maximum Full-Scale Output Current	I_{FS_max}	—		30	—	mA
CMOS Input Logic High	V_{IH}	LOGIC PORT	V_{IOVDD} = 3.3 V	2.4	—	V
			V_{IOVDD} = 1.8 V	1.5	—	V
CMOS Input Logic Low	V_{IL}		V_{IOVDD} = 3.3 V	—	0.4	V
			V_{IOVDD} = 1.8 V	—	0.3	V
LVDS Input Voltage Range	$V_{LVDSCOM}$	DATA、DCI		1.0	1.4	V
LVDS Input Differential Threshold	$\|V_{IDTH}\|$			200	—	mV
LVDS Differential Input Impedance	R_{IN}			75	135	Ω
DAC Clock Input Differential Peak-to-Peak Voltage	V_{CLKTH}	DACCLKP、DACCLKN		0.4	1.8	V
Output Compliance Range	V_{OC}	—		-1	+1	V
AVDD33	I_{AVDD33}	f_{dac} =1000MSPS, f_{out} =10MHz		—	75	mA
CVDD18	I_{CVDD18}	f_{dac} =1000MSPS, f_{out} =10MHz		—	115	mA
DVDD18	I_{DVDD18}	f_{dac} =1000MSPS, f_{out} =10MHz		—	560	mA
Power Consumption	P_W	f_{dac} =1000MSPS, f_{out} =10MHz		—	1.5	W
Power Supply Rejection Ratio	*PSRR*	V_{AVDD33}		-5	+5	%FSR/V
Maximum Clock Rate	f_{DAC}	—		1.0	—	GSPS

Parameter	Symbol	Test Condition (V_{IOVDD}=V_{AVDD33} = 3.3 V、V_{CVDD18} = V_{DVDD18} =1.8 V、I_{OUTFS} = 20 mA、-55℃ ≤ T_A≤ 125℃)	Min	Max	Unit
Spurious-Free Dynamic Range	*SFDR*	f_{dac} =100MSPS，f_{out}=20MHz	72	—	dBc
		f_{dac} =200MSPS，f_{out}=50MHz	66	—	dBc
		f_{dac} =400MSPS，f_{out}=70MHz	63	—	dBc
		f_{dac} =1000MSPS，f_{out}=20MHz	70	—	dBc
		f_{dac} =1000MSPS，f_{out}=70MHz	55	—	dBc
Two-Tone Intermodulation Distortion	*IMD*	f_{dac} =200MSPS，f_{out}=50MHz	68	—	dBc

Table 5-2 Absolute Maximum Ratings

AVDD33 to AVSS, EPAD, CVSS, DVSS	−0.3 V to +3.6 V
IOVDD to AVSS, EPAD, CVSS, DVSS	−0.3 V to +3.6 V
DVDD18, CVDD18 to AVSS, EPAD, CVSS, DVSS	−0.3 V to +2.1 V
AVSS to EPAD, CVSS, DVSS	−0.3 V to +0.3 V
EPAD to AVSS, CVSS, DVSS	−0.3 V to +0.3 V
CVSS to AVSS, EPAD, DVSS	−0.3 V to +0.3 V
DVSS to AVSS, EPAD, CVSS	−0.3 V to +0.3 V
FSADJ, REFIO, IOUT1P, IOUT1N, IOUT2P, IOUT2N to AVSS	−0.3 V to AVDD33 + 0.3 V
D[15:0]P, D[15:0]N, FRAMEP, FRAMEN, DCIP, DCIN to EPAD, DVSS	−0.3 V to DVDD18 + 0.3 V
DACCLKP, DACCLKN, REFCLKP, REFCLKN to CVSS	−0.3 V to CVDD18 + 0.3 V
$\overline{RESET}$, $\overline{IRQ}$, $\overline{CS}$, SCLK, SDIO, SDO to EPAD, DVSS	−0.3 V to IOVDD + 0.3 V
Junction Temperature	175 ℃
Storage Temperature Range	−65 ℃ to +150 ℃

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6. Pin configuration and function descriptions

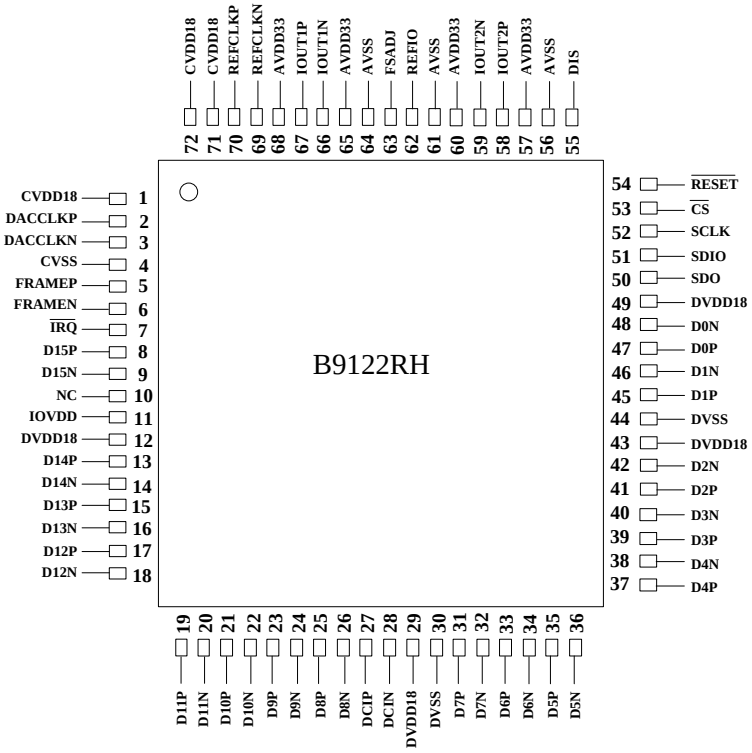


Figure 6-1 Pin Descriptions

Table 6-1. Pin Function Descriptions

Pin	Symbol	Description
1	CVDD18	1.8 V Clock Supply. Supplies clock receivers, clock distribution, and PLL circuitry.
2	DACCLKP	DAC Clock Input, Positive.
3	DACCLKN	DAC Clock Input, Negative.
4	CVSS	Clock Supply Common.
5	FRAMEP	Frame Input, Positive. This pin must be tied to DVSS if not used.
6	FRAMEN	Frame Input, Negative. This pin must be tied to DVDD18 if not used.
7	$\overline{\text{IRQ}}$	Interrupt Request. Open-drain, active low output. Connect an external pull-up to IOVDD through a 10 kΩ resistor.
8	D15P	Data Bit 15 (MSB), Positive.
9	D15N	Data Bit 15 (MSB), Negative.
10	NC	No Connect. Do not connect to this pin.
11	IOVDD	Supply Pin for Serial Port I/O Pins, $\overline{\text{RESET}}$, and $\overline{\text{IRQ}}$. 1.8 V to 3.3 V can be supplied to this pin.
12	DVDD18	1.8 V Digital Supply. Supplies power to digital core and digital data ports.
13	D14P	Data Bit 14, Positive.
14	D14N	Data Bit 14, Negative.
15	D13P	Data Bit 13, Positive.

Pin	Symbol	Description
16	D13N	Data Bit 13, Negative.
17	D12P	Data Bit 12, Positive.
18	D12N	Data Bit 12, Negative.
19	D11P	Data Bit 11, Positive.
20	D11N	Data Bit 11, Negative.
21	D10P	Data Bit 10, Positive.
22	D10N	Data Bit 10, Negative.
23	D9P	Data Bit 9, Positive.
24	D9N	Data Bit 9, Negative.
25	D8P	Data Bit 8, Positive.
26	D8N	Data Bit 8, Negative.
27	DCIP	Data Clock Input, Positive.
28	DCIN	Data Clock Input, Negative.
29	DVDD18	1.8 V Digital Supply. Supplies power to digital core and digital data ports.
30	DVSS	Digital Common.
31	D7P	Data Bit 7, Positive.
32	D7N	Data Bit 7, Negative.
33	D6P	Data Bit 6, Positive.
34	D6N	Data Bit 6, Negative.
35	D5P	Data Bit 5, Positive.
36	D5N	Data Bit 5, Negative.
37	D4P	Data Bit 4, Positive.
38	D4N	Data Bit 4, Negative.
39	D3P	Data Bit 3, Positive.
40	D3N	Data Bit 3, Negative.
41	D2P	Data Bit 2, Positive.
42	D2N	Data Bit 2, Negative.
43	DVDD18	1.8 V Digital Supply. Supplies power to digital core and digital data ports.
44	DVSS	Digital Common.
45	D1P	Data Bit 1, Positive.
46	D1N	Data Bit 1, Negative.
47	D0P	Data Bit 0 (LSB), Positive.
48	D0N	Data Bit 0 (LSB), Negative.
49	DVDD18	1.8 V Digital Supply. Supplies power to digital core and digital data ports.
50	SDO	Serial Port Data Output (CMOS Levels with Respect to IOVDD).
51	SDIO	Serial Port Data Input/Output (CMOS Levels with Respect to IOVDD).
52	SCLK	Serial Port Clock Input (CMOS Levels with Respect to IOVDD).
53	$\overline{CS}$	Serial Port Chip Select, Active Low (CMOS Levels with Respect to IOVDD).
54	$\overline{RESET}$	Reset, Active Low (CMOS Levels with Respect to IOVDD).
55	DIS	Serial Port disable test, Active High, Normally connected to AVSS.
56	AVSS	Analog Supply Common.

Pin	Symbol	Description
57	AVDD33	3.3 V Analog Supply.
58	IOUT2P	Q DAC Positive Current Output.
59	IOUT2N	Q DAC Negative Current Output.
60	AVDD33	3.3 V Analog Supply.
61	AVSS	Analog Supply Common.
62	REFIO	Voltage Reference. Nominally 1.2 V output. Should be decoupled to AVSS.
63	FSADJ	Full-Scale Current Output Adjust. Place a 10 kΩ resistor from this pin to AVSS.
64	AVSS	Analog Supply Common.
65	AVDD33	3.3 V Analog Supply.
66	IOUT1N	I DAC Negative Current Output.
67	IOUT1P	I DAC Positive Current Output.
68	AVDD33	3.3 V Analog Supply.
69	REFCLKN	PLL Reference Clock Input, Negative. This pin has a secondary function as a synchronization input.
70	REFCLKP	PLL Reference Clock Input, Positive. This pin has a secondary function as a synchronization input.
71	CVDD18	1.8 V Clock Supply. Supplies clock receivers, clock distribution, and PLL circuitry.
72	CVDD18	1.8 V Clock Supply. Supplies clock receivers, clock distribution, and PLL circuitry.
	EPAD	The exposed pad (EPAD) must be soldered to the ground plane (AVSS). The EPAD provides an electrical, thermal, and mechanical connection to the board.

7. Product Description

The B9122RH combines many features that make it a very attractive DAC for wired and wireless communications systems. The dual digital signal path and dual DAC structure allow an easy interface to common quadrature modulators when designing single side-band (SSB) transmitters. The speed and performance of the B9122RH allow wider bandwidths and more carriers to be synthesized than in previously available DACs. In addition, the B9122RH includes an innovative low power, 32-bit, complex NCO that greatly increases the ease of frequency placement.

The B9122RH offers features that allow simplified synchronization with incoming data and between multiple devices. Auxiliary DACs are also provided on chip. The auxiliary DACs can be used for output dc offset compensation (for LO compensation in SSB transmitters) and for gain matching (for image rejection optimization in SSB transmitters).

7.0 Serial Port Operation

The serial port is a flexible, synchronous serial communications port that allows easy interfacing to many industry-standard micro-controllers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including both the Motorola SPI and Intel® SSR protocols. The interface allows read/write access to all registers that configure the B9122RH. Single-byte or multiple-byte transfers are supported, as well as MSB first or LSB first transfer formats. The serial port interface can be configured as a single-pin I/O (SDIO) or as two unidirectional pins for input and output (SDIO and SDO).

A communication cycle with the B9122RH has two phases. Phase 1 is the instruction cycle (the writing of an instruction byte into the device), coincident with the first eight SCLK rising edges. The instruction byte provides the serial port controller with information regarding the data transfer cycle—Phase 2 of the communication cycle. The Phase 1 instruction byte defines whether the upcoming data transfer is a read or write, along with the starting register address for the first byte of the data transfer. The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the device.

A logic high on the $\overline{CS}$ pin followed by a logic low resets the serial port timing to the initial state of the instruction cycle. From this state, the next eight rising SCLK edges represent the instruction bits of the current I/O operation.

The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the device and the system controller. Phase 2 of the communication cycle is a transfer of one or more data bytes. Registers change immediately upon writing to the last bit of each transfer byte, except for the frequency tuning word and NCO phase offsets, which change only when the frequency tuning word (FTW) update bit (Register 0x36, Bit 0) is set.

The instruction byte contains the information shown in Table 7-0.

Table 7-0.Serial Port Instruction Byte

I7 (MSB)	I6	I5	I4	I3	I2	I1	I0(LSB)
R/W	A6	A5	A4	A3	A2	A1	A0

R/W, Bit 7 of the instruction byte, determines whether a read or a write data transfer occurs after the instruction byte write. Logic 1 indicates a read operation, and Logic 0 indicates a write operation. A6 to A0, Bit 6 to Bit 0 of the instruction byte,

determine the register that is accessed during the data transfer portion of the communication cycle. For multibyte transfers, A6 is the starting byte address. The remaining register addresses are generated by the device based on the LSB_FIRST bit (Register 0x00, Bit 6).

SCLK

The serial clock pin synchronizes data to and from the device and runs the internal state machines. The maximum frequency of SCLK is 40 MHz. All data input is registered on the rising edge of SCLK. All data is driven out on the falling edge of SCLK.

$\overline{CS}$

An active low input starts and gates a communication cycle. It allows more than one device to be used on the same serial communications lines. When the $\overline{CS}$ pin is high, the SDO and SDIO pins go to a high impedance state. During the communica-tion cycle, the $\overline{CS}$ pin should stay low.

SDIO

Data is always written into the device on this pin. However, this pin can be used as a bidirectional data line. The configuration of this pin is controlled by Register 0x00, Bit 7. The default is Logic 0, configuring the SDIO pin as unidirectional.

SDO

Data is read from this pin for protocols that use separate lines for transmitting and receiving data. If the device operates in a single bidirectional I/O mode, this pin does not output data and is set to a high impedance state.

7.1 Serial Port Options

The serial port can support both MSB first and LSB first data formats. This functionality is controlled by the LSB_FIRST bit (Register 0x00, Bit 6). The default is MSB first (LSB_FIRST = 0).

When LSB_FIRST = 0 (MSB first), the instruction and data bits must be written from MSB to LSB. Multibyte data transfers in MSB first format start with an instruction byte that includes the register address of the most significant data byte. Subsequent data bytes should follow from high address to low address. In MSB first mode, the serial port internal byte address generator decrements for each data byte of the multibyte communication cycle.

When LSB_FIRST = 1 (LSB first), the instruction and data bits must be written from LSB to MSB. Multibyte data transfers in LSB first format start with an instruction byte that includes the register address of the least significant data byte. Subsequent data bytes should follow from low address to high address. In LSB first mode, the serial port internal byte address generator increments for each data byte of the multibyte communication cycle.

If the MSB first mode is active, the serial port controller data address decrements from the data address written toward 0x00 for multibyte I/O operations. If the LSB first mode is active, the serial port controller data address increments from the data address written toward 0x7F for multibyte I/O operations.

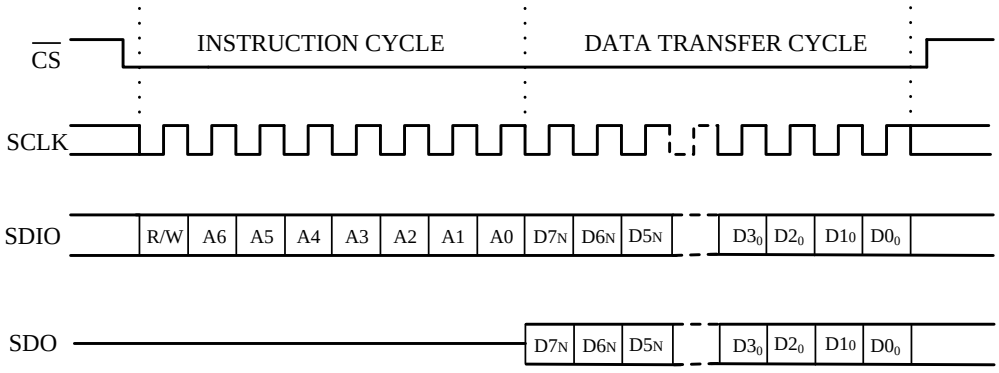


Figure 7-1. Serial Port Interface Timing, MSB First

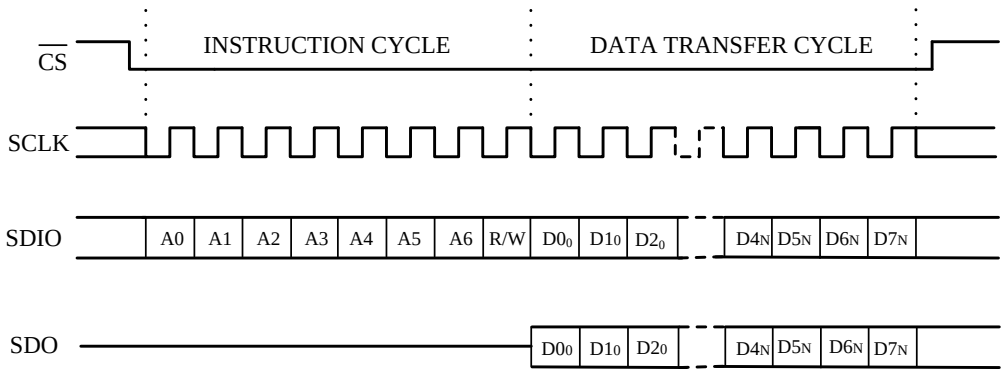


Figure 7-2. Serial Port Interface Timing, LSB First

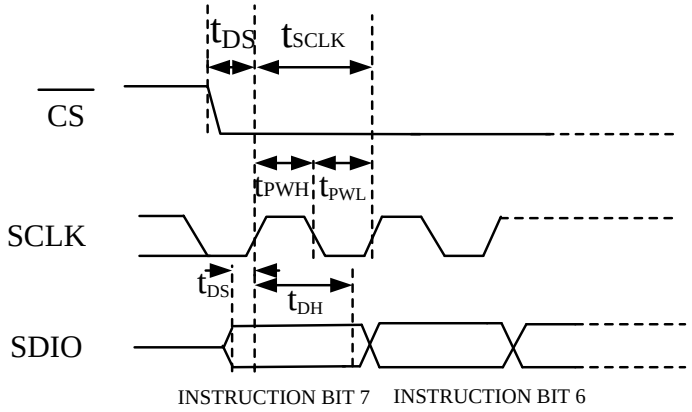


Figure 7-3. Timing Diagram for Serial Port Register Write

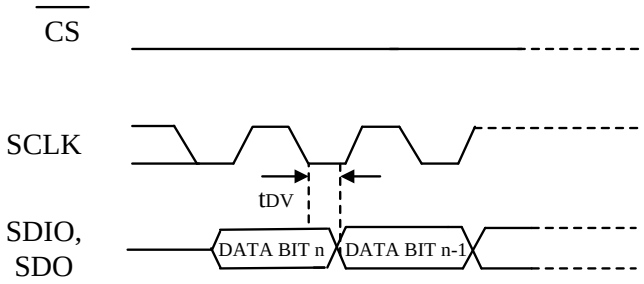


Figure 7-4. Timing Diagram for Serial Port Register Read

7.2 Device Configuration Register Map and Descriptions

Table 7-1 Device Configuration Register Map

Addr (Hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
0x00	Comm	SDIO	LSB_FIRST	Reset						0x00
0x01	Power control	Power down I DAC	Power down Q DAC	Power down data receiver	Power down aux ADC					0x10
0x03	Data format	Binary data format	Q data first	MSB swap				Data Bus Width[1:0]		0x00
0x04	Interrupt enable	Enable PLL lock lost	Enable PLL locked	Enable sync signal lost	Enable sync signal locked			Enable FIFO Warning 1	Enable FIFO Warning 2	0x00
0x05	Interrupt enable	0	0	0	Enable AED compare pass	Enable AED compare fail	Enable SED compare fail	0	0	0x00
0x06	Event flag	PLL lock lost	PLL locked	Sync signal lost	Sync signal locked			FIFO Warning 1	FIFO Warning 2	NA

Addr (Hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
0x07	Event flag				AED compare pass	AED compare fail	SED compare fail			NA
0x08	Clock receiver control	DACCLK duty correction	REFCLK duty correction	DACCLK cross-correction	REFCLK cross-correction	1	1	1	1	0x3F
0x0A	PLL control	PLL enable	PLL manual enable	Manual VCO Band[5:0]						0x40
0x0C	PLL control	PLL Loop Bandwidth[1:0]			PLL Charge Pump Current[4:0]					0xD1
0x0D	PLL control	N2[1:0]			PLL cross-control enable	N0[1:0]		N1[1:0]		0xD9
0x0E	PLL status	PLL locked				VCO Control Voltage[3:0]				NA
0x0F	PLL status			VCO Band Readback[5:0]						NA
0x10	Sync control	Sync enable	Data/FIFO rate toggle			Rising edge sync	Sync Averaging[2:0]			0x48
0x11	Sync control			Sync Phase Request[5:0]						0x00
0x12	Sync status	Sync lost	Sync locked							NA
0x13	Sync status	Sync Phase Readback[7:0] (6.2 format)								NA
0x15	Data receiver status			LVDS FRAME level high	LVDS FRAME level low	LVDS DCI level high	LVDS DCI level low	LVDS data level high	LVDS data level low	NA
0x16	DCI delay							DCI Delay[1:0]		0x00
0x17	FIFO control						FIFO Phase Offset[2:0]			0x04
0x18	FIFO status	FIFO Warning 1	FIFO Warning 2				FIFO soft align ack	FIFO soft align request		NA
0x19	FIFO status	FIFO Level[7:0]								NA
0x1B	Datapath control	Bypass premod	Bypass sinc−1	Bypass NCO		NCO gain	Bypass phase	Select sideband	Send I data to	0xE4

Addr (Hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
							comp and dc offset		Q data	
0x1C	HB1 control						HB1[1:0]		Bypass HB1	0x00
0x1D	HB2 control		HB2[5:0]						Bypass HB2	0x00
0x1E	HB3 control		HB3[5:0]						Bypass HB3	0x00
0x1F	Chip ID	Chip ID[7:0]								0x08
0x30	FTW LSB	FTW[7:0]								0x00
0x31	FTW	FTW[15:8]								0x00
0x32	FTW	FTW[23:16]								0x00
0x33	FTW MSB	FTW[31:24]								0x00
0x34	NCO phase offset LSB	NCO Phase Offset[7:0]								0x00
0x35	NCO phase offset MSB	NCO Phase Offset[15:8]								0x00
0x36	NCO FTW update			FRAME FTW ack	FRAME FTW request			Update FTW ack	Update FTW request	0x00
0x38	I phase adj LSB	I Phase Adj[7:0]								0x00
0x39	I phase adj MSB							I Phase Adj[9:8]		0x00
0x3A	Q phase adj LSB	Q Phase Adj[7:0]								0x00
0x3B	Q phase adj MSB							Q Phase Adj[9:8]		0x00
0x3C	I DAC offset LSB	I DAC Offset[7:0]								0x00
0x3D	I DAC offset MSB	I DAC Offset[15:8]								0x00
0x3E	Q DAC	Q DAC Offset[7:0]								0x00

Addr (Hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
	offset LSB									
0x3F	Q DAC offset MSB	Q DAC Offset[15:8]								0x00
0x40	I DAC FS adjust	I DAC FS Adj[7:0]								0xF9
0x41	I DAC control	I DAC sleep						I DAC FSAdj[9:8]		0x01
0x42	I aux DAC data	I Aux DAC[7:0]								0x00
0x43	I aux DAC control	I aux DAC sign	I aux DAC current direction	I aux DAC sleep				I Aux DAC[9:8]		0x00
0x44	Q DAC FS adjust	Q DAC FS Adj[7:0]								0xF9
0x45	Q DAC control	Q DAC sleep						QDAC FS Adj[9:8]		0x01
0x46	Q aux DAC data	Q Aux DAC[7:0]								0x00
0x47	Qaux DAC control	Q aux DAC sign	Qaux DAC current direction	Q aux DAC sleep				Q Aux DAC[9:8]		0x00
0x48	Die temp range control		FS Current[2:0]			Reference Current[2:0]			Capacitor value	0x02
0x49	Die temp LSB	Die Temp[7:0]								NA
0x4A	Die temp MSB	Die Temp[15:8]								NA
0x67	SED control	SED compare enable		Sample error detected		Autoclear enable		Compare fail	Compare pass	0x00
0x68	Compare	Compare Value I0[7:0]								0xB6

Addr (Hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
	I0 LSBs									
0x69	Compare I0 MSBs	Compare Value I0[15:8]								0x7A
0x6A	Compare Q0 LSBs	Compare Value Q0[7:0]								0x45
0x6B	Compare Q0 MSBs	Compare Value Q0[15:8]								0xEA
0x6C	Compare I1 LSBs	Compare Value I1[7:0]								0x16
0x6D	Compare I1 MSBs	Compare Value I1[15:8]								0x1A
0x6E	Compare Q1 LSBs	Compare Value Q1[7:0]								0xC6
0x6F	Compare Q1 MSBs	Compare Value Q1[15:8]								0xAA
0x70	SED I LSBs	Errors Detected I_BITS[7:0]								0x00
0x71	SED I MSBs	Errors Detected I_BITS[15:8]								0x00
0x72	SED Q LSBs	Errors Detected Q_BITS[7:0]								0x00
0x73	SED Q MSBs	Errors Detected Q_BITS[15:8]								0x00
0x7F	Revision	0	0	Revision[3:0]			0		0	NA

Table 7-2. Device Configuration Register Descriptions

Register	Address	Bits	Name	Description	Default
Comm	0x00	7	SDIO	SDIO pin operation. 0 = SDIO operates as an input only. 1 = SDIO operates as a bidirectional input/output.	0
		6	LSB_FIRST	Serial port communication, LSB or MSB first. 0 = MSB first. 1 = LSB first.	0
		5	Reset	The device is placed in reset when this bit is written high and remains in reset until the bit is	0

Register	Address	Bits	Name	Description	Default
				written low.	
Power Control	0x01	7	Power down I DAC	1 = power down I DAC.	0
		6	Power down Q DAC	1 = power down Q DAC.	0
		5	Power down data receiver	1 = power down the input data receiver.	0
		4	Power down auxiliary ADC	1 = power down the auxiliary ADC for temperature sensor.	1
Data Format	0x03	7	Binary data format	0 = input data is in twos complement format. 1 = input data is in binary format.	0
		6	Q data first	Indicates I/Q data pairing on data input. 0 = I data sent to data receiver first. 1 = Q data sent to data receiver first.	0
		5	MSB swap	Swaps the bit order of the data input port. 0 = order of the data bits corresponds to the pin descriptions. 1 = bit designations are swapped; most significant bits become the least significant bits.	0
		[1:0]	Data Bus Width[1:0]	Data receiver interface mode. See the LVDS Input Data Ports section for information about the operation of the different interface modes. 00 = word mode; 16-bit interface bus width. 01 = byte mode; 8-bit interface bus width. 10 = nibble mode; 4-bit interface bus width. 11 = invalid.	00
Interrupt Enable	0x04	7	Enable PLL lock lost	1 = enable interrupt for PLL lock lost.	0
		6	Enable PLL locked	1 = enable interrupt for PLL	0

Register	Address	Bits	Name	Description	Default
				locked.	
		5	Enable sync signal lost	1 = enable interrupt for sync signal lost.	0
		4	Enable sync signal locked	1 = enable interrupt for sync signal locked.	0
		1	Enable FIFO Warning 1	1 = enable interrupt for FIFO Warning 1.	0
		0	Enable FIFO Warning 2	1 = enable interrupt for FIFO Warning 2.	0
Interrupt Enable	0x05	[7:5]	Set to 0	Set these bits to 0.	000
		4	EnableAEDcomparepass	1 = enable interrupt for AED comparison pass.	0
		3	Enable AED compare fail	1 = enable interrupt for AED comparison fail.	0
		2	Enable SED compare fail	1 = enable interrupt for SED comparison fail.	0
		[1:0]	Set to 0	Set these bits to 0.	00
Event Flag	0x06	7	PLL lock lost	1 = indicates that the PLL, which had been previouslylocked, has unlocked from the reference signal. This is a latched signal.	NA
		6	PLL locked	1 = indicates that the PLL has locked to the reference clock input.	NA
		5	Sync signal lost	1 = indicates that the sync logic, which had been previously locked, has lost alignment. This is a latched signal.	NA
		4	Sync signal locked	1 = indicates that the sync logic has achieved sync alignment. This is indicated when no phase changes were requested for at least a few full averaging cycles.	NA
		1	FIFO Warning 1	1 = indicates that the difference between the FIFO read and write pointers is 1.	NA
		0	FIFO Warning 2	1 = indicates that the difference between the FIFO read and write pointers is 2.	NA
			Note that all event flags are cleared by writing the		

Register	Address	Bits	Name	Description	Default
			respective bit high.		
	0x07	4	AED compare pass	1 = indicates that the SED logic detected a valid input data pattern compared against the preprogrammed expected values. This is a latched signal.	NA
		3	AED compare fail	1 = indicates that the SED logic detected an invalid input data pattern compared against the preprogrammed expected values. This latched signal is automatically clearedwhen eight valid I/Q data pairs are received.	NA
		2	SED compare fail	1 = indicates that the SED logic detected an invalid input data pattern compared against the preprogrammed expected values. This is a latched signal.	NA
			Note that all event flags are cleared by writing the respective bit high.		
Clock ReceiverControl	0x08	7	DACCLK duty correction	1 = enable dutycycle correction on the DACCLK input.	0
		6	REFCLK duty correction	1 = enable dutycycle correction on the REFCLK input.	0
		5	DACCLK cross-correction	1 = enable differential crossing correction on the DACCLK input.	1
		4	REFCLK cross-correction	1 = enable differential crossing correction on the REFCLK input.	1
PLL Control	0x0A	7	PLL enable	1 = enable the PLL clock multiplier. The REFCLK input is used as the PLL reference clock signal.	0
		6	PLL manual enable	1 = enable manual selection of the VCO band. The correct VCO band must be determined by the user and written to Bits[5:0].	1
		[5:0]	Manual VCO Band[5:0]	Selects the VCO band to be used.	000000

Register	Address	Bits	Name	Description	Default
	0x0C	[7:6]	PLL Loop Bandwidth[1:0]	Selects the PLL loop filter bandwidth. 00 = widest bandwidth. … 11 = narrowest bandwidth.	11
		[4:0]	PLL Charge PumpCurrent[4:0]	Sets the nominal PLL charge pump current.00000 = lowest current setting. … 11111 = highest current setting.	10001
PLL Control	0x0D	[7:6]	N2[1:0]	PLL control clock divider. This divider determines the ratio of the DACCLK frequency to the PLL controller clock frequency. fPC_CLK must always be less than 75 MHz. 00 = fDACCLK/fPC_CLK = 2. 01 = fDACCLK/fPC_CLK = 4. 10 = fDACCLK/fPC_CLK = 8. 11 = fDACCLK/fPC_CLK = 16.	11
		4	PLL cross-control enable	1 = enable PLL cross-point controller.	1
		[3:2]	N0[1:0]	PLL VCO divider. This divider determines the ratio of the VCO frequency to the DACCLK frequency. 00 = fVCO/fDACCLK = 1. 01 = fVCO/fDACCLK = 2. 10 = fVCO/fDACCLK = 4. 11 = fVCO/fDACCLK = 4.	10
		[1:0]	N1[1:0]	PLL loop divider. This divider determines the ratio of the DACCLK frequency to the REFCLK frequency. 00 = fDACCLK/fREFCLK = 2. 01 = fDACCLK/fREFCLK = 4. 10 = fDACCLK/fREFCLK = 8. 11 = fDACCLK/fREFCLK = 16.	01
PLL Status	0x0E	7	PLL locked	1 = the PLL-generated clock is tracking the REFCLK input signal.	NA
		[3:0]	VCO Control Voltage[3:0]	VCO control voltage readback.	NA
	0x0F		VCO Band	Indicates the VCO band	NA

Register	Address	Bits	Name	Description	Default
		[5:0]	Readback[5:0]	currently selected.	
Sync Control	0x10	7	Sync enable	1 = enable the synchronization logic.	0
		6	Data/FIFO rate toggle	0 = operate the synchronization at the FIFO reset rate. 1 = operate the synchronization at the data rate.	1
		3	Rising edge sync	0 = sync is initiated on the falling edge of the sync input. 1 = sync is initiated on the rising edge of the sync input.	1
		[2:0]	Sync Averaging[2:0]	Sets the number of input samples that are averaged in determining the sync phase. 000 = 1. 001 = 2. 010 = 4. 011 = 8. 100 = 16. 101 = 32. 110 = 64. 111 = 128.	000
	0x11	[5:0]	Sync Phase Request[5:0]	This register sets the requested clock phase offset after sync. The offset unit is in DACCLK cycles. This register enables repositioning of the DAC output with respect to the sync input. The offset can also be used to skew the DAC outputs between the synchronized DACs. 000000 = 0 DACCLK cycles. 000001 = 1 DACCLK cycle. … 111111 = 63 DACCLK cycles.	000000
Sync Status	0x12	7	Sync lost	1 = synchronization was attained but has been lost.	NA
		6	Sync locked	1 = synchronization has been attained.	NA
	0x13	[7:0]	Sync Phase Readback[7:0]	Indicates the averaged sync phase offset (6.2 format). If this value differs from the Sync	NA

Register	Address	Bits	Name	Description	Default
				Phase Request[5:0] value in Register 0x11, a sync timing error has occurred. For more information, see the Sync Status Bits section. 00000000 = 0.0. 00000001 = 0.25. … 11111110 = 63.50. 11111111 = 63.75.	
Data Receiver Status	0x15	5	LVDS FRAME level high	One or both LVDS FRAME input signals have exceeded 1.7 V.	NA
		4	LVDS FRAME level low	One or both LVDS FRAME input signals have crossed below 0.7 V.	NA
		3	LVDS DCI level high	One or both LVDS DCI input signals have exceeded 1.7 V.	NA
		2	LVDS DCI level low	One or both LVDS DCI input signal have crossed below 0.7 V	NA
		1	LVDS data level high	One or more LVDS Dx input signals have exceeded 1.7 V.	NA
		0	LVDS data level low	One or more LVDS Dx input signal have crossed below 0.7 V	NA
DCI Delay	0x16	[1:0]	DCI Delay[1:0]	This option is available for the Revision 2 silicon only. The DCI delay bits control the delay applied to the DCI signal. The DCI delay affects the sampling interval of the DCI with respect to the Dx inputs. 00 = 350 ps delay of DCI signal. 01 = 590 ps delay of DCI signal. 10 = 800 ps delay of DCI signal. 11 = 925 ps delay of DCI signal.	00
FIFO Control	0x17	[2:0]	FIFO Phase Offset[2:0]	FIFO write pointer phase offset following FIFO reset. This is the difference between the read pointer and the write pointer values upon FIFO reset. The optimal value is nominally 4 (100). 000 = 0.	100

Register	Address	Bits	Name	Description	Default
				001 = 1. … 111 = 7.	
FIFO Status	0x18	7	FIFO Warning 1	1 = FIFO read and write pointers are within ±1.	NA
		6	FIFO Warning 2	1 = FIFO read and write pointers are within ±2.	NA
		2	FIFO soft align acknowledge	1 = FIFO read and write pointers are aligned after a serial port initiated FIFO reset.	NA
		1	FIFO soft align request	1 = request FIFO read and write pointer alignment via the serial port.	0
	0x19	[7:0]	FIFO Level[7:0]	Thermometer encoded measure of the FIFO level.	NA
Datapath Control	0x1B	7	Bypass premod	1 = bypass the fS/2 premodulator.	1
		6	Bypass sinc−1	1 = bypass the inverse sinc filter.	1
		5	Bypass NCO	1 = bypass the NCO.	1
		3	NCO gain	0 = no gain scaling is applied to the NCO input to the internal digital modulator (default). 1 = gain scaling of 0.5 is applied to the NCO input to the internal digital modulator. Gain scaling can eliminate satu-ration of the modulator output for some combinations of data inputs and NCO signals.	0
		2	Bypass phase compensation and dc offset	1 = bypass phase compensation and dc offset.	1

Register	Address	Bits	Name	Description	Default
		1	Select sideband	0 = the modulator outputs the high-side image. 1 = the modulator outputs the low-side image. The image is spectrally inverted compared to the input data.	0
		0	Send I data to Q data	1 = ignore Q data from the interface and disable the clocks to the Q datapath. Send I data to both the I and Q DACs.	0
HB1 Control	0x1C	[2:1]	HB1[1:0]	Modulation mode for I Side Half-Band Filter 1. 00 = input signal not modulated; filter pass band is from -0.4 to +0.4 of fIN1. 01 = input signal not modulated; filter pass band is from 0.1 to 0.9 of fIN1. 10 = input signal modulated by fIN1; filter pass band is from 0.6 to 1.4 of fIN1. 11 = input signal modulated by fIN1; filter pass band is from 1.1 to 1.9 of fIN1.	00
		0	Bypass HB1	1 = bypass the first-stage interpolation filter.	0
HB2 Control	0x1D	[6:1]	HB2[5:0]	Modulation mode for I Side Half-Band Filter 2. 000000 = input signal not modulated; filter pass band is from −0.25 to +0.25 of fIN2. 001001 = input signal not modulated; filter pass band is from 0.0 to 0.5 of fIN2. 010010 = input signal not modulated; filter pass band is from 0.25 to 0.75 of fIN2. 011011 = input signal not modulated; filter pass band is from 0.5 to 1.0 of fIN2. 100100 = input signal modulated by fIN2; filter pass	000000

Register	Address	Bits	Name	Description	Default
				band is from 0.75 to 1.25 of fIN2. 101101 = input signal modulated by fIN2; filter pass band is from 1.0 to 1.5 of fIN2. 110110 = input signal modulated by fIN2; filter pass band is from 1.25 to 1.75 of fIN2. 111111 = input signal modulated by fIN2; filter pass band is from 1.5 to 2.0 of fIN2.	
		0	Bypass HB2	1 = bypass the second-stage interpolation filter.	0
HB3 Control	0x1E	[6:1]	HB3[5:0]	Modulation mode for I Side Half-Band Filter 3. 000000 = input signal not modulated; filter pass band is from -0.2 to +0.2 of fIN3. 001001 = input signal not modulated; filter pass band is from 0.05 to 0.45 of fIN3. 010010 = input signal not modulated; filter pass band is from 0.3 to 0.7 of fIN3. 011011 = input signal not modulated; filter pass band is from 0.55 to 0.95 of fIN3. 100100 = input signal modulated by fIN3; filter pass band is from 0.8 to 1.2 of fIN3. 101101 = input signal modulated by fIN3; filter pass band is from 1.05 to 1.45 of fIN3. 110110 = input signal modulated by fIN3; filter pass band is from 1.3 to 1.7 of fIN3. 111111 = input signal modulated by fIN3; filter pass band is from 1.55 to 1.95 of fIN3.	000000

Register	Address	Bits	Name	Description	Default
		0	Bypass HB3	1 = bypass the third-stage interpolation filter.	0
Chip ID	0x1F	[7:0]	Chip ID[7:0]	This register identifies the device as an B9122RH.	00001000
FTW LSB	0x30	[7:0]	FTW[7:0]	See Register 0x33.	00000000
FTW	0x31	[7:0]	FTW[15:8]	See Register 0x33.	00000000
FTW	0x32	[7:0]	FTW[23:16]	See Register 0x33.	00000000
FTW MSB	0x33	[7:0]	FTW[31:24]	FTW[31:0] is the 32-bit frequency tuning word that deter-mines the frequency of the complex carrier generated by the on-chip NCO. The frequency is not updated when the FTW registers are written. The values are only updated when Bit 0 of Register 0x36 transitions from 0 to 1.	00000000
NCO Phase Offset LSB	0x34	[7:0]	NCO Phase Offset[7:0]	See Register 0x35.	00000000
NCO Phase Offset MSB	0x35	[7:0]	NCO Phase Offset[15:8]	The NCO sets the phase of the complex carrier signal when the NCO is reset. The phase offset spans from 0 °to 360 °. Each bit represents an offset of 0.0055 °. This value is in twos complement format.	00000000
NCO FTW Update	0x36	5	FRAME FTW acknowledge	1 = the NCO has been reset due to an extended FRAME pulse signal.	0
		4	FRAME FTW request	0 = the NCO is reset on the first extended FRAME pulse after this bit is set to 1.	0
		1	Update FTW acknowledge	1 = the FTW has been updated.	0
		0	Update FTW request	The FTW is updated on the 0-to-1 transition of this bit.	0
I Phase Adj	0x38	[7:0]	I Phase Adj[7:0]	See Register 0x39.	00000000

Register	Address	Bits	Name	Description	Default
LSB					
I Phase Adj MSB	0x39	[1:0]	I Phase Adj[9:8]	I Phase Adj[9:0] is used to insert a phase offset between the I and Q datapaths. This offset can be used to correct for phase imbalance in a quadrature modulator. See the Quadrature Phase Correction section for more information.	00
Q Phase Adj LSB	0x3A	[7:0]	Q Phase Adj[7:0]	See Register 0x3B.	00000000
Q Phase Adj MSB	0x3B	[1:0]	Q Phase Adj[9:8]	Q Phase Adj[9:0] is used to insert a phase offset between the I and Q datapaths. This offset can be used to correct for phase imbalance in a quadrature modulator. See the Quadrature Phase Correction section for more information.	00
I DAC Offset LSB	0x3C	[7:0]	I DAC Offset[7:0]	See Register 0x3D.	00000000
I DAC Offset MSB	0x3D	[7:0]	I DAC Offset[15:8]	I DAC Offset[15:0] is a value that is added directly to the samples written to the I DAC.	00000000
Q DAC Offset LSB	0x3E	[7:0]	Q DAC Offset[7:0]	See Register 0x3F.	00000000
Q DAC Offset MSB	0x3F	[7:0]	Q DAC Offset[15:8]	Q DAC Offset[15:0] is a value that is added directly to the samples written to the Q DAC.	00000000
I DAC FS Adjust	0x40	[7:0]	I DAC FS Adj[7:0]	See Register 0x41, Bits[1:0].	11111001
I DAC Control	0x41	7	I DAC sleep	1 = puts the I DAC into sleep mode (fast wake-up mode).	0
		[1:0]	I DAC FS Adj[9:8]	I DAC FS Adj[9:0] sets the full-scale current of the I DAC. The full-scale current can be adjusted from 8.64 mA to 31.68 mA in step sizes of	01

Register	Address	Bits	Name	Description	Default
				approximately 22.5 µA. 0x000 = 8.64 mA. … 0x200 = 20.16 mA. … 0x3FF = 31.68 mA.	
I Aux DAC Data	0x42	[7:0]	I Aux DAC[7:0]	See Register 0x43, Bits[1:0].	00000000
I Aux DAC Control	0x43	7	I aux DAC sign	0 = the I auxiliary DAC sign is positive, and the current is directed to the IOUT1P pin (Pin 67). 1 = the I auxiliary DAC sign is negative, and the current is directed to the IOUT1N pin (Pin 66).	0
		6	I aux DAC current direction	0 = the I auxiliary DAC sources current. 1 = the I auxiliary DAC sinks current.	0
		5	I aux DAC sleep	1 = puts the I auxiliary DAC into sleep mode.	0
		[1:0]	I Aux DAC[9:8]	I Aux DAC[9:0] sets the magnitude of the auxiliary DACcurrent. The range is 0 mA to 2 mA, and the step size is 2 µA.0x000 = 0.000 mA. 0x001 = 0.002 mA. … 0x3FF = 2.046 mA.	00
Q DAC FS Adjust	0x44	[7:0]	Q DAC FS Adj[7:0]	See Register 0x45, Bits[1:0].	11111001
Q DAC Control	0x45	7	Q DAC sleep	1 = puts the Q DAC into sleep mode (fast wake-up mode).	0
		[1:0]	Q DAC FS Adj[9:8]	Q DAC FS Adj[9:0] sets the full-scale current of the Q DAC. The full-scale current can be adjusted from 8.64 mA to 31.68 mA in step sizes of approximately 22.5 µA. 0x000 = 8.64 mA. … 0x200 = 20.16 mA. … 0x3FF = 31.68 mA.	01
Q Aux DAC Data	0x46	[7:0]	Q Aux DAC[7:0]	See Register 0x47, Bits[1:0].	00000000

Register	Address	Bits	Name	Description	Default
Q Aux DAC Control	0x47	7	Q aux DAC sign	0 = the Q auxiliary DAC sign is positive, and the current is directed to the IOUT2P pin (Pin 58). 1 = the Q auxiliary DAC sign is negative,and the current is directed to the IOUT2N pin (Pin 59).	0
		6	Q aux DAC current direction	0 = the Q auxiliary DAC sources current.1 = the Q auxiliary DAC sinks current.	0
		5	Q aux DAC sleep	1 = puts the Q auxiliary DAC into sleep mode.	0
		[1:0]	Q Aux DAC[9:8]	Q Aux DAC[9:0]sets the magnitude of the auxiliary DAC current. The range is 0 mA to 2 mA, and the step size is 2 µA.0x000 = 0.000 mA. 0x001 = 0.002 mA. … 0x3FF = 2.046 mA.	00
Die Temp RangeControl	0x48	[6:4]	FS Current[2:0]	Auxiliary ADC full-scale current.000 = lowest current.… 111 = highest current.	000
		[3:1]	Reference Current[2:0]	Auxiliary ADC reference current.000 = lowest current.… 111 = highest current.	001
		0	Capacitor value	Auxiliary ADC internal capacitor value.0 = 5 pF.1 = 10 pF.	0
Die Temp LSB	0x49	[7:0]	Die Temp[7:0]	See Register 0x4A.	N/A
Die Temp MSB	0x4A	[7:0]	Die Temp[15:8]	Die Temp[15:0] indicates the approximate die temperature. For more information, see the Temperature Sensor section.	N/A
SED Control	0x67	7	SED compare enable	1 = enable the SED circuitry. None of the flags in this register or the values in Register 0x70 through Register 0x73 are significant if the SED is not enabled.	0

Register	Address	Bits	Name	Description	Default
		5	Sample error detected	1 = indicates an error was detected. The bit remains set until cleared. Any write to this register clears this bit to 0.	0
		3	Autoclear enable	1 = enable autoclear mode. This activates Bit 1 and Bit 0 of this register and causes Register 0x70 through Register 0x73 to be autocleared when eight consecutive sample data sets are received error free.	0
		1	Compare fail	1 = indicates an error was detected. This bit remains set until it is autocleared by the reception of eight consecutive error-free comparisons or is cleared by a write to this register.	0
		0	Compare pass	1 = indicates that the last sample comparison was error free.	0
CompareI0 LSBs	0x68	[7:0]	Compare Value I0[7:0]	See Register 0x69.	10110110
CompareI0 MSBs	0x69	[7:0]	Compare Value I0[15:8]	Compare Value I0[15:0] is the word that is compared with the I0 input sample captured at the input interface.	01111010
CompareQ0 LSBs	0x6A	[7:0]	Compare Value Q0[7:0]	See Register 0x6B.	01000101
CompareQ0 MSBs	0x6B	[7:0]	Compare Value Q0[15:8]	Compare Value Q0[15:0] is the word that is compared with the Q0 input sample captured at the input interface.	11101010
CompareI1 LSBs	0x6C	[7:0]	Compare Value I1[7:0]	See Register 0x6D.	00010110
CompareI1 MSBs	0x6D	[7:0]	Compare Value I1[15:8]	Compare Value I1[15:0] is the word that is compared with the I1 input sample captured at the input interface.	00011010
Compare Q1 LSBs	0x6E	[7:0]	Compare Value Q1[7:0]	See Register 0x6F.	11000110

Register	Address	Bits	Name	Description	Default
Compare Q1 MSBs	0x6F	[7:0]	Compare Value Q1[15:8]	Compare Value Q1[15:0] is the word that is compared with the Q1 input sample captured at the input interface.	10101010
SED I LSBs	0x70	[7:0]	Errors Detected I_BITS[7:0]	See Register 0x71.	00000000
SED I MSBs	0x71	[7:0]	Errors Detected I_BITS[15:8]	Errors Detected I_BITS[15:0] indicates which bits were received in error.	00000000
SED Q LSBs	0x72	[7:0]	Errors Detected Q_BITS[7:0]	See Register 0x73.	00000000
SED Q MSBs	0x73	[7:0]	Errors Detected Q_BITS[15:8]	Errors Detected Q_BITS[15:0] indicates which bits were received in error.	00000000
Revision	0x7F	[5:2]	Revision[3:0]	This value corresponds to the die revision number. 0001 = Die Revision 1. 0011 = Die Revision 2.	NA

Notice

Note that in the radiation condition, all registers that configure the B9122RH should be refreshed.

7.3 Theory of Operation

7.3.1 LVDS Input Data Ports

The B9122RH has one LVDS data port that receives data for both the I and Q transmit paths. The device can accept data in word, byte, and nibble formats. In word, byte, and nibble modes, the data is sent over 16-bit, 8-bit, and 4-bit LVDS data buses, respectively. The pin assignments of the bus in each mode are shown in Table 7-3.

Table 7-3 Data Bit Pair Assignments for Data Input Modes

Mode	MSB to LSB
Word	D15, D14, …, D0
Byte	D14, D12, D10, D8, D7, D5, D3, D1
Nibble	D10, D8, D7, D5

In byte and nibble modes, the unused pins can be left floating.

The data is accompanied by a reference bit (DCI) that is used to generate a double data rate (DDR) clock. In byte and nibble modes, a FRAME signal is required for controlling to which DAC the data is sent. All of the interface signals are time aligned, so there is a maximum skew requirement on the bus.

7.3.1.1 Word Interface Mode

In word mode, the DCI signal is a reference bit used to generate the data sampling clock. The DCI signal should be time aligned with the data. The I DAC data should correspond to DCI high, and the Q DAC data should correspond to DCI low, as shown in Figure 7-5.

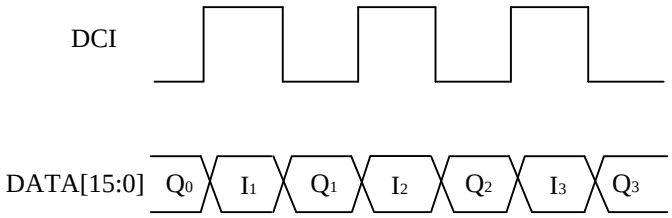


Figure 7-5. Timing Diagram for Word Mode

7.3.1.2 Byte Interface Mode

In byte mode, the DCI signal is a reference bit used to generate the data sampling clock. The DCI signal should be time aligned with the data. The most significant byte of the data should correspond to DCI high, and the least significant byte of the data should correspond to DCI low. The FRAME signal indicates to which DAC the data is sent. When FRAME is high, data is sent to the I DAC; when FRAME is low, data is sent to the Q DAC. The complete timing diagram is shown in Figure 7-6.

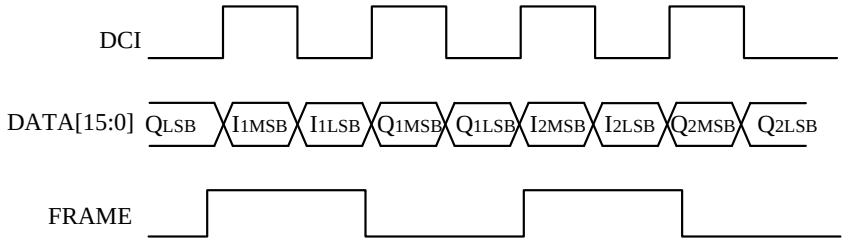


Figure 7-6. Timing Diagram for Byte Mode

7.3.1.3 Nibble Interface Mode

In nibble mode, the DCI signal is a reference bit used to generate the data sampling clock. The DCI signal should be time aligned with the data. The FRAME signal indicates to which DAC the data is sent. When FRAME is high, data is sent to the I DAC; when FRAME is low, data is sent to the Q DAC. All four nibbles must be written to the device for proper operation. For 12-bit resolution devices, the data in the fourth nibble acts as a place-holder for the data framing structure. The complete

timing diagram is shown in Figure 7-7.

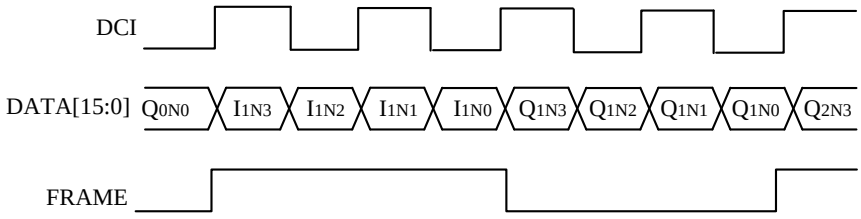


Figure 7-7. Timing Diagram for Nibble Mode

7.3.1.4 Interface Timing

The timing diagram for the digital interface port is shown in Figure 7-8. The sampling point of the data bus nominally occurs 350 ps after each edge of the DCI signal and has an uncertainty of ±300 ps, as illustrated by the sampling interval shown in Figure 7-8. The data and FRAME signals must be valid through-out this sampling interval. The data and FRAME signals may change at any time between sampling intervals. The setup (t_S) and hold (t_H) times, with respect to the edges, are shown in Figure 7-8. The minimum setup and hold times are shown in Table 7-4.

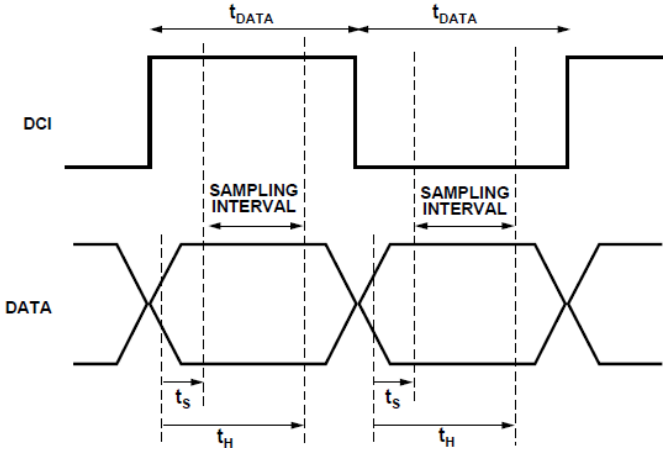


Figure 7-8. Timing Diagram for Input Data Port

Table 7-4 Data to DCI Setup and Hold Times

DCI Delay Register 0x16, Bits[1:0]	Minimum Setup Time, t_S(ns)	Minimum Hold Time, t_H(ns)	Sampling Interval(ns)
00	−0.05	0.65	0.6
01	−0.23	0.95	0.72
10	−0.38	1.22	0.84
11	−0.47	1.38	0.91

7.3.1.5 FIFO Operation

The B9122RH contains a 2-channel, 16-bit wide, eight-word deep FIFO designed

to relax the timing relationship between the data arriving at the DAC input ports and the internal DAC data rate clock. The FIFO acts as a buffer that absorbs timing variations between the data source and the DAC, such as the clock-to-data variation of an FPGA or ASIC, which significantly increases the timing budget of the interface.

Figure 7-9 shows the block diagram of the datapath through the FIFO. The data is latched into the device, is formatted, and is then written into the FIFO register determined by the FIFO write pointer. The value of the write pointer is incremented every time a new word is loaded into the FIFO. Meanwhile, data is read from the FIFO register determined by the read pointer and fed into the digital datapath. The value of the read pointer is incremented every time data is read into the datapath from the FIFO. The FIFO pointers are incremented at the data rate (DACCLK rate divided by the interpolation ratio).

Valid data is transmitted through the FIFO as long as the FIFO does not overflow or become empty. An overflow or empty condition of the FIFO occurs when the write pointer and read pointer point to the same FIFO location. This simultaneous access of data leads to unreliable data transfer through the FIFO and must be avoided.

Nominally, data is written to and read from the FIFO at the same rate. This keeps the FIFO depth constant. If data is written to the FIFO faster than data is read out, the FIFO depth increases. If data is read out of the FIFO faster than data is written to it, the FIFO depth decreases. For optimum timing margin, the FIFO depth should be maintained near half full (a difference of 4 between the write pointer and read pointer values). The FIFO depth represents the FIFO pipeline delay and is part of the over-all latency of the B9122RH.

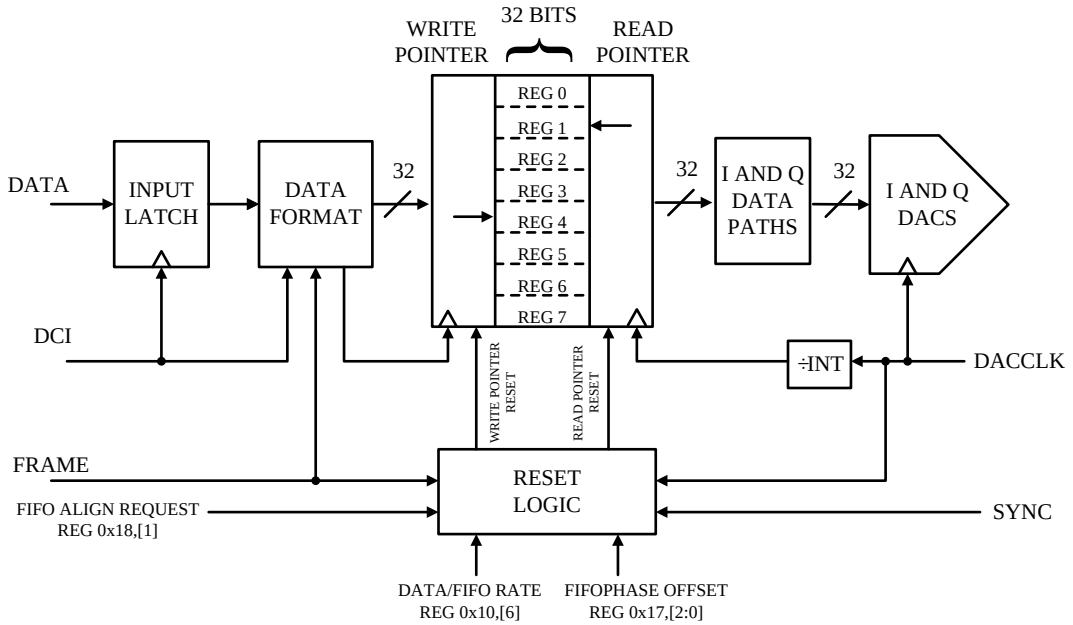


Figure 7-9. FIFO Block Diagram

When the B9122RH is powered on, the FIFO depth is unknown. To avoid a concurrent read and write to the same FIFO address and to ensure a fixed pipeline delay, it is important to reset the FIFO pointers to known states. The FIFO pointers can be initialized in two ways: via a write sequence to the serial port or by strobing the FRAME input. There are two types of FIFO resets: a relative reset and an absolute reset. A relative reset enforces a defined FIFO depth. An absolute reset enforces a particular write pointer value when the reset is initiated. A serial port initiated FIFO reset is always a relative reset. A FRAME strobe initiated reset can be either a relative or an absolute reset.

If the FRAME differential inputs are not used for FIFO reset or for framing the word width, they must be tied to logic low. FRAMEP must be tied to DVSS, and FRAMEN must be tied to DVDD18 to avoid accidental reset of the FIFO due to noise.

The operation of the FRAME initiated FIFO reset depends on the synchronization mode chosen.

• When synchronization is disabled or when it is configured for data rate mode synchronization, the FRAME strobe initiates a relative FIFO reset. The reference point of the relative reset is the position of the read pointer.

• When FIFO mode synchronization is chosen, the FRAME strobe initiates an absolute FIFO reset.

For more information about the synchronization function, see the Multichip

Synchronization section.

A summary of the synchronization modes and the types of FIFO reset used is provided in Table 7-5.

Table 7-5 Summary of FIFO Resets

FIFO Reset Signal	Synchronization Mode		
	Disabled	Data Rate	FIFO Reset
Serial Port	Relative	Relative	Relative
FRAME	Relative	Relative	Absolute

Serial Port Initiated FIFO Reset

A serial port initiated FIFO reset can be issued in any synchronization mode and always results in a relative FIFO reset. To initialize the FIFO data level through the serial port, Bit 1 of Register 0x18 should be toggled from 0 to 1 and back. When the write to this register is complete, the FIFO data level is initialized. When the initialization is triggered, the next time that the read pointer becomes 0, the write pointer is set to the value of the FIFO start level variable (Register 0x17, Bits[2:0]) upon initialization. By default, this value is 4, but it can be programmed to a value from 0 to 7. It is recommended that a value of 5 (0x05) be programmed in Register 0x17.

The recommended procedure for a serial port FIFO data level initialization is as follows:

1. Program Register 0x17 to 0x05.
2. Request FIFO level reset by setting Register 0x18, Bit 1, to 1.
3.Verify that the part acknowledges the request by ensuring that Register 0x18, Bit 2, is set to 1.
4.Remove the request by setting Register 0x18, Bit 1, to 0.
5.Verify that the part drops the acknowledge signal by ensuring that Register 0x18, Bit 2, is set to 0.
6.Read back Register 0x19 to verify that the pointer spacing is set to 3 (0x07) or 4 (0x0F).
7.If the readback of Register 0x19 shows a pointer spacing of 2 (0x03), increment Register 0x17 to a spacing of 0x06 and repeat Step 2 through Step 5. Read back Register 0x19 again to verify that the pointer spacing is now set to 3 (0x07).
8. If the readback of Register 0x19 shows a pointer spacing of 5 (0x1F) after Step 6, decrement Register 0x17 to a spacing of 0x04 and repeat Step 2 through Step 5. Read back Register 0x19 again to verify that the pointer spacing is now set to 4 (0x0F).

FRAME Initiated Relative FIFO Reset

The primary function of the FRAME input is to indicate to which DAC the input data is written. Another function of the FRAME input is to initialize the FIFO data level value. This is done by asserting the FRAME signal high for at least the time interval required to load complete data to the I and Q DACs. This corresponds to one DCI period in word mode, two DCI periods in byte mode, and four DCI periods in nibble mode.

To initiate a relative FIFO reset with the FRAME signal, the device must be configured in data rate mode (Register 0x10, Bit 6 = 1). When FRAME is asserted in data rate mode, the write pointer is set to 4 by default (or to the FIFO start level) the next time that the read pointer becomes 0.

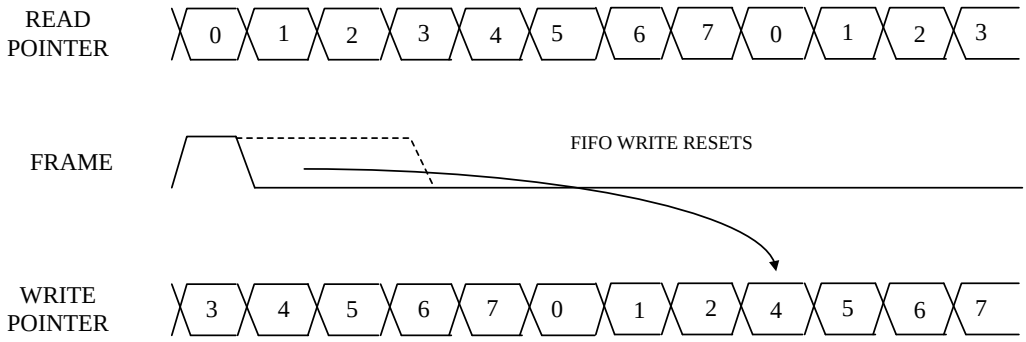


Figure 7-10. FRAME Input vs. Write Pointer Value, Data Rate Mode

FRAME Initiated Absolute FIFO Reset

In FIFO rate synchronization mode, the write pointer of the FIFO is reset in an absolute manner. The synchronization signal aligns the internal clocks on the part to a common reference clock so that the pipeline delay in the digital circuit stays the same during power cycles. The synchronization signal is sampled by the DAC clock in the B9122RH. The edge of the DAC clock used to sample the synchronization signal is selected by Bit 3 of Register 0x10.

The FRAME signal is used to reset the FIFO write pointer. In the FIFO rate synchronization mode, the FIFO write pointer is reset immediately after the FRAME signal is asserted high for at least the time interval required to load complete data to the I and Q DACs. The FIFO write pointer is reset to the value of the FIFO Phase Offset[2:0] bits in Register 0x17. FIFO rate synchro-nization is selected by setting Bit 6 of Register 0x10 to 0.

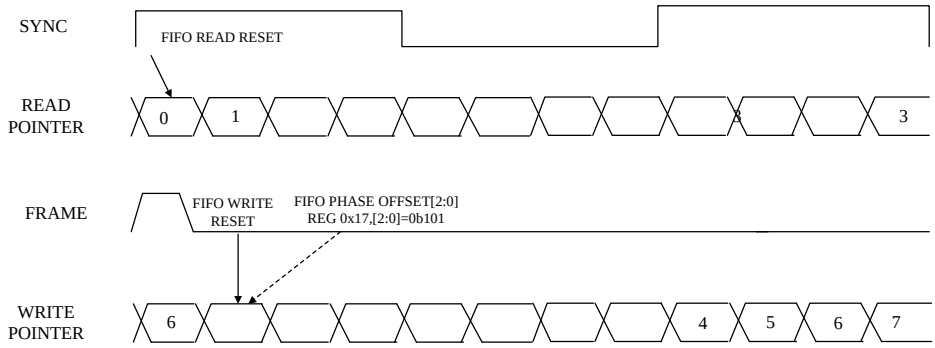


Figure 7-11. F0RAME Input vs. Write Pointer Value, FIFO Rate Mode

Monitoring the FIFO Status

The FIFO initialization and status can be read from Register 0x18. This register provides information about the FIFO status and whether the initialization was successful. The MSB of Register 0x18 is a FIFO warning flag that can optionally trigger a device $\overline{\text{IRQ}}$. This flag indicates that the FIFO is close to emptying (FIFO level is 1) or overflowing (FIFO level is 7). In this case, data may soon be corrupted, and action should be taken.

The FIFO data level can be read from Register 0x19 at any time. The serial port reported FIFO data level is denoted as a 7-bit thermometer code (Base 1 code) of the write counter state relative to the absolute read counter being at 0. The optimum FIFO data level of 4 is therefore reported as a value of 00001111 in the status register.

Note that, depending on the timing relationship between the DCI and the main DACCLK, the FIFO level value can be off by a ±1 count, that is, the readback of Register 0x19 can be 00011111 in the case of a +1 count and 00000111 in the case of a -1 count. Therefore, it is important to keep the difference between the read and write pointers to a value of at least 2.

7.3.2 Digital Data Path

The block diagram in the Figure 7-12 shows the functionality of the digital data path. The digital processing includes a premodulation block, three half-band (HB) interpolation filters, a quadrature modulator with a fine resolution NCO, phase and offset adjustment blocks, and an inverse sinc filter.

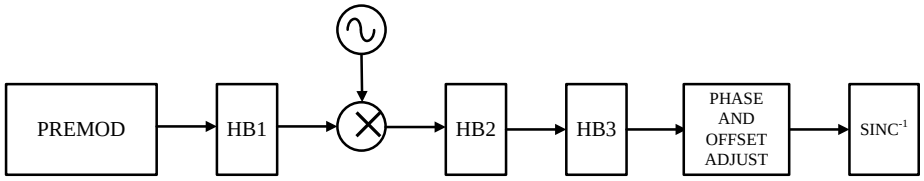


Figure 7-12. Block Diagram of Digital Data Path

The digital data path accepts I and Q data streams and processes them as a quadrature data stream. The signal processing blocks can be used when the input data stream is represented as complex data.

The digital data path can also be used to process an input data stream representing two independent real data streams, but the functionality is somewhat restricted. The premodulation block and any of the non-shifted interpolation filter modes can be used for an input data stream representing two independent real data streams. See the Coarse Modulation Mixing Sequences section for more information.

7.3.2.1 Premodulation

The half-band interpolation filters have selectable pass bands that allow the center frequencies to be moved in increments of one-half their input data rate. The premodulation block provides a digital upconversion of the incoming waveform by one-half the incoming data rate, f_{DATA}. This can be used to frequency-shift base-band input data to the center of the interpolation filter pass band.

7.3.2.2 Interpolation Filters

The transmit path contains three interpolation filters. Each of the three interpolation filters provides a 2× increase in output data rate. The half-band (HB) filters can be individually bypassed or cascaded to provide 1×, 2×, 4×, or 8× interpolation ratios. Each half-band filter stage offers a different combination of bandwidths and operating modes.

The bandwidth of the three half-band filters with respect to the data rate at the filter input is as follows:

Bandwidth of HB1 = 0.8 × fIN1

Bandwidth of HB2 = 0.5 × fIN2

Bandwidth of HB3 = 0.4 × fIN3

The filters have a pass-band ripple of less than ±0.001 dB and an image rejection of greater than 50dB.

7.3.2.3 NCO Modulation

The digital quadrature modulator makes use of a numerically controlled oscillator (NCO), a phase shifter, and a complex modulator to provide a means for modulating the signal by a programmable carrier signal. A block diagram of the digital modulator

is shown in Figure 7-13. The fine modulation provided by the digital modulator, in conjunction with the coarse modulation of the interpolation filters and premodulation block, allows the signal to be placed anywhere in the output spectrum with very fine frequency resolution.

The quadrature modulator is used to mix the carrier signal generated by the NCO with the I and Q signal. The NCO produces a quadrature carrier signal to translate the input signal to a new center frequency. A complex carrier signal is a pair of sinusoidal waveforms of the same frequency, offset 90 ° from each other. The frequency of the complex carrier signal is set via FTW[31:0] in Register 0x30 through Register 0x33.

The NCO operating frequency, f_{NCO}, is at either f_{DATA} (HB1 bypassed) or $2 \times f_{DATA}$ (HB1 enabled). The frequency of the complex carrier signal can be set from dc up to f_{NCO}. The frequency tuning word (FTW) is calculated as

$$FTW = \frac{f_{CARRIER}}{f_{NCO}} \times 2^{32}$$

The generated quadrature carrier signal is mixed with the I and Q data. The quadrature products are then summed into the I and Q data paths, as shown in Figure 7-13.

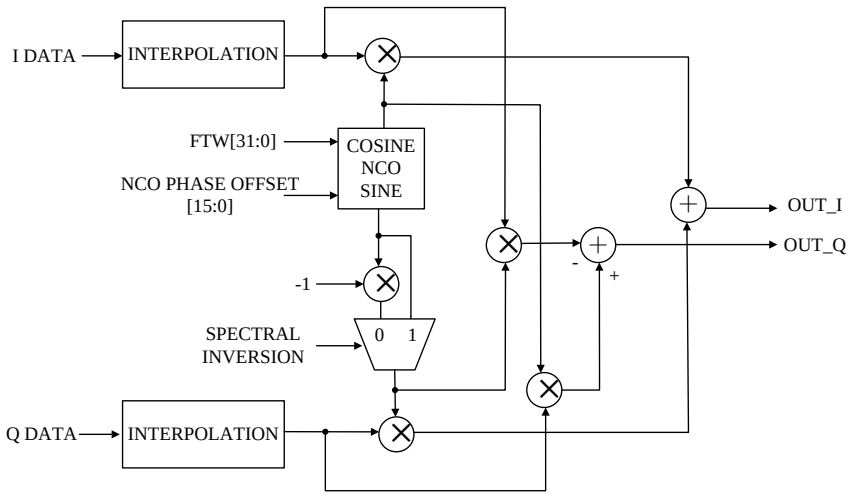


Figure 7-13. Digital Quadrature Modulator Block Diagram

The frequency tuning word registers are not updated immediately upon writing, as other configuration registers are. After loading the FTW registers with the desired values, Bit 0 of Register 0x36 must transition from 0 to 1 for the new FTW to take effect.

7.3.2.4 Quadrature Phase Correction

The purpose of the quadrature phase correction block is to enable compensation of the phase imbalance of the analog quadrature modulator following the DAC. If the quadrature modulator has a phase imbalance, the unwanted sideband appears with significant energy. Tuning the quadrature phase adjust value can optimize image rejection in single sideband radios.

Ordinarily, the I and Q channels have an angle of precisely 90 °between them. The quadrature phase adjustment is used to change the angle between the I and Q channels. When I Phase Adj[9:0] (Register 0x38 and Register 0x39) is set to 1000000000, the I DAC output moves approximately 1.75 ° away from the Q DAC output, creating an angle of 91.75 °between the channels. When I Phase Adj[9:0] is set to 0111111111, the I DAC output moves approximately 1.75 ° toward the Q DAC output, creating an angle of 88.25 °between the channels.

Q Phase Adj[9:0] (Register 0x3A and Register 0x3B) works in a similar fashion. When Q Phase Adj[9:0] is set to 1000000000, the Q DAC output moves approximately 1.75 ° away from the I DAC output, creating an angle of 91.75 ° between the channels. When Q Phase Adj[9:0] is set to 0111111111, the Q DAC output moves approximately 1.75 ° toward the I DAC output, creating an angle of 88.25 °between the channels.

Based on these two endpoints, the combined resolution of the phase compensation register is approximately 3.5 ⁰⁄1024 or 0.00342 °per code.

7.3.3 DAC Input Clock Configurations

The B9122RH DAC sampling clock (DACCLK) can be sourced directly or by clock multiplying. Clock multiplying uses the on-chip phase-locked loop (PLL), which accepts a reference clock operating at a submultiple of the desired DACCLK rate, most commonly the data input frequency. The PLL then multiplies the reference clock up to the desired DACCLK frequency, which can then be used to generate all the internal clocks required by the DAC. The clock multiplier provides a high quality clock that meets the performance requirements of most applications. Using the on-chip clock multiplier eliminates the need to generate and distribute the high speed DACCLK.

The second mode bypasses the clock multiplier circuitry and allows the DACCLK to be sourced directly to the DAC core. This mode enables the user to source a very high quality clock directly to the DAC core. Sourcing the DACCLK directly through the REFCLKP, REFCLKN, DACCLKP, and DACCLKN pins may be necessary in

demanding applications that require the lowest possible DAC output noise, particularly when directly synthesizing signals above 150 MHz.

7.3.3.1 Driving The DACCLK and REFCLK Inputs

The differential DACCLK and REFCLK inputs share similar clock receiver input circuitry. Figure 7-14 shows a simplified circuit diagram of the inputs. The on-chip clock receiver has a differential input impedance of about 10 kΩ. It is self-biased to a common-mode voltage of about 1.25 V. The inputs can be driven by direct coupling differential PECL or LVDS drivers. The inputs can also be ac-coupled if the driving source cannot meet the input compliance voltage of the receiver.

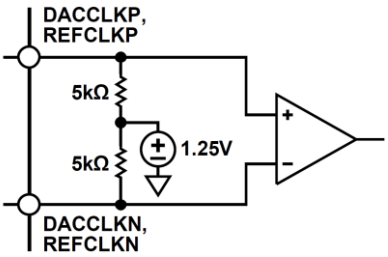


Figure 7-14. Clock Receiver Input Simplified Equivalent Circuit

The minimum input drive level to either of the clock inputs is 200 mV p-p differential. The optimal performance is achieved

when the clock input signal is between 800 mV p-p differential and 1.6 V p-p differential. Whether using the on-chip clock multiplier or sourcing the DACCLK directly, it is necessary that the input clock signal to the device have low jitter and fast edge rates to optimize the DAC noise performance.

7.3.3.2 Direct Clocking

Direct clocking with a low noise clock produces the lowest noise spectral density at the DAC outputs. To select the differential CLK inputs as the source for the DAC sampling clock, set the PLL enable bit (Register 0x0A, Bit 7) to 0. This powers down the internal PLL clock multiplier and selects the input from the DACCLKP and DACCLKN pins as the source for the internal DAC sampling clock.

The device also has duty cycle correction circuitry and differential input level correction circuitry. Enabling these circuits can provide improved performance in some cases. The control bits for these functions are in Register 0x08.

7.3.3.3 Clock Multiplication

The on-chip PLL clock multiplication circuit can be used to generate the DAC sampling clock from a lower frequency reference clock. When the PLL enable bit (Register 0x0A, Bit 7) is set to 1, the clock multiplication circuit generates the DAC sampling clock from the lower rate REFCLK input. The functional diagram of the clock multiplier is shown in Figure 7-15.

The clock multiplication circuit operates such that the VCO outputs a frequency, f_{VCO}, equal to the REFCLK input signal frequency multiplied by N1 × N0.

$$f_{VCO} = f_{REFCLK} \times (N1 \times N0)$$

The DAC sampling clock frequency, f_{DACCLK}, is equal to

$$f_{DACCLK} = f_{REFCLK} \times N1$$

The output frequency of the VCO must be chosen to keep f_{VCO} in the optimal operating range of 1.0 GHz to 2.1 GHz. The frequency of the reference clock and the values of N1 and N0 must be chosen so that the desired DACCLK frequency can be synthesized and the VCO output frequency is in the correct range.

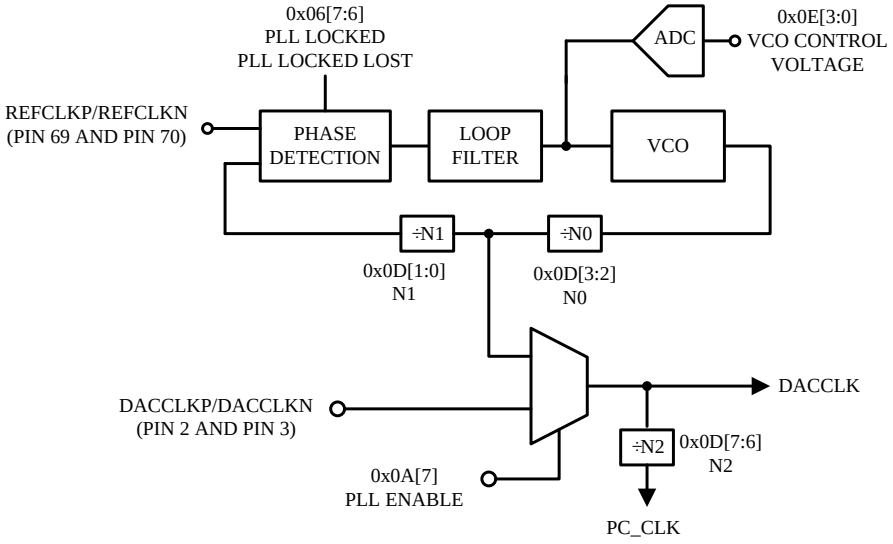


Figure 7-15. PLL Clock Multiplication Circuit

7.3.3.4 PLL Settings

Three settings for the PLL circuitry should be programmed to their nominal values. The PLL values shown in Table 7-14 are the recommended settings for these parameters.

Table 7-14 PLL Setting

PLL Control Register	Register Address	Bits	Optimal Setting
PLL Loop Bandwidth[1:0]	0x0C	[7:6]	11
PLL Charge Pump Current[4:0]	0x0C	[4:0]	10001
PLL Cross-Control Enable	0x0D	4	1

7.3.3.5 Configuring The VCO Tuning Band

The PLL VCO has a valid operating range from approximately 1.0 GHz to 2.1 GHz covered in 63 overlapping frequency bands. For any desired VCO output frequency, there may be several valid PLL band select values. The frequency bands of a typical device are shown in Figure 7-16. Device-to-device variations and operating temperature affect the actual band frequency range. Therefore, it is required that the optimal PLL band select value be determined for each individual device.

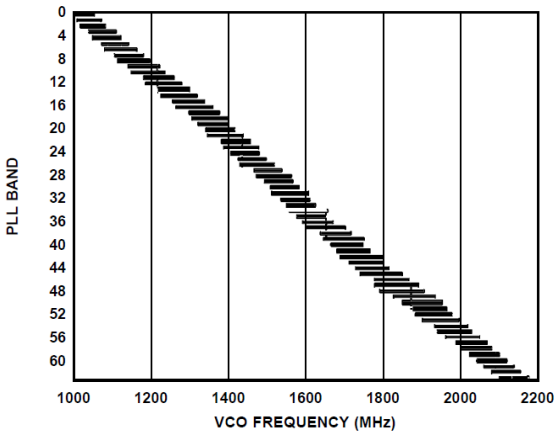


Figure 7-16. PLL Lock Range over Temperature for a Typical Device

7.3.3.6 Automatic VCO Band Select

The device has an automatic VCO band select feature on chip. Using the automatic VCO band select feature is a simple and reliable method of configuring the VCO frequency band. This feature is enabled by starting the PLL in manual mode, then placing the PLL in auto band select mode. This is done by setting Register 0x0A to a value of 0xCF, then to a value of 0xA0. When these values are written, the device executes an automated routine that determines the optimal VCO band setting for the device.

7.3.3.7 Manual VCO Band Select

The device also has a manual band select mode (PLL manual enable, Register 0x0A, Bit 6 = 1) that allows the user to select the VCO tuning band. In manual mode, the VCO band is set directly with the value written to the manual VCO band bits (Register 0x0A, Bits[5:0]). To properly select the VCO band, follow these steps:

1. Put the device in manual band select mode by setting Register 0x0A, Bit 6 = 1.

2. Sweep the VCO band over a range of bands that results in the PLL being locked.

3. For each band, verify that the PLL is locked and read the PLL using the VCO control voltage bits (Register 0x0E, Bits[3:0]).

4. Select the band that results in the control voltage being closest to the center of the range, that is, 1001 or 1000. The resulting VCO band should be the optimal setting for the device. Write this value to the manual VCO band bits (Register 0x0A, Bits[5:0]).

5. If desired, an indication of where the VCO is within the operating frequency band can be determined by querying the VCO control voltage. Table 7-15 shows how to interpret the PLL VCO control voltage value (Register 0x0E, Bits[3:0]).

Table 7-15. VCO Control Voltage Range Indications

VCO Control Voltage (Register 0x0E, Bits[3:0])	Indication
1111 1110	Move to higher VCO band
1101 1100 1011 1010	VCO is operating in the higher end of the frequency band
1001 1000 0111 0110	VCO is operating within an optimal region of the frequency band
0101 0100 0011 0010	VCO is operating in the lower end of the frequency band
0001 0000	Move to lower VCO band

7.3.4 Analog Outputs

7.3.4.1 Transmit DAC Operation

Figure 7-17 shows a simplified block diagram of the transmit path DACs. The

DAC core consists of a current source array, a switch core, digital control logic, and full-scale output current control. The DAC full-scale output current (IFS) is nominally 20 mA. The output currents from the IOUT1P/IOUT2P and IOUT1N/ IOUT2N pins are complementary, meaning that the sum of the two currents always equals the full-scale current of the DAC. The digital input code to the DAC determines the effective differential current delivered to the load.

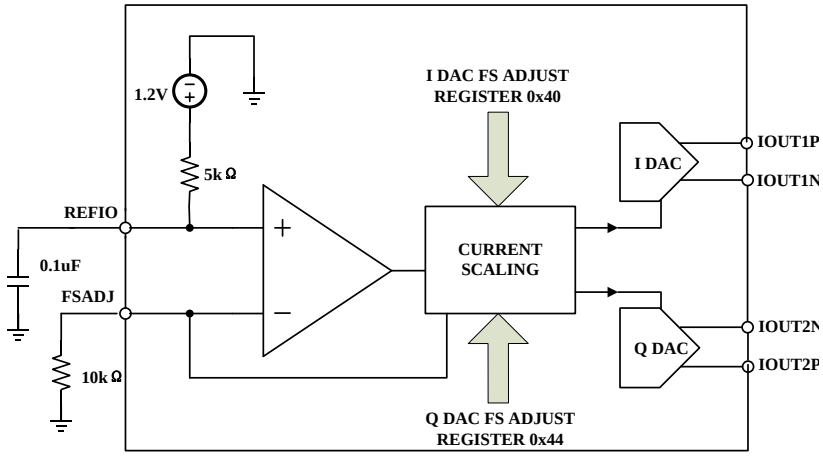


Figure 7-17. Simplified Block Diagram of DAC Core

The DAC has a 1.2 V band gap reference with an output impedance of 5 kΩ. The reference output voltage appears on the REFIO pin. When using the internal reference, decouple the REFIO pin to AVSS with a 0.1 µF capacitor. Use the internal reference only for external circuits that draw dc currents of 2 µA or less. For dynamic loads or static loads greater than 2 µA, buffer the REFIO pin. If desired, the internal reference can be overdriven by applying an external reference (from 1.10 V to 1.30 V) to the REFIO pin. A 10 kΩ external resistor, RSET, must be connected from the FSADJ pin to AVSS. This resistor, along with the reference control amplifier, sets up the correct internal bias currents for the DAC. Because the full-scale current is inversely proportional to this resistor, the tolerance of RSET is reflected in the full-scale output amplitude. The full-scale current equation, where the DAC gain is set individually for the I and Q DACs in Register 0x40 and Register 0x44, respectively, is as follows:

$$I_{FS} = \frac{V_{REF}}{R_{SET}} \times \left(72 + (\frac{3}{16} \times DACgain) \right)$$

For the nominal values of VREF (1.2 V), RSET (10 kΩ), and DAC gain (512), the full-scale current of the DAC is typically 20.16 mA. The DAC full-scale current can be adjusted from 8.64 mA to 31.68 mA by setting the DAC gain parameter, as shown

in Figure 7-18.

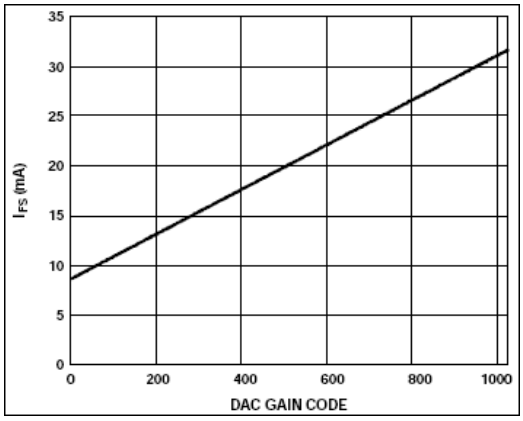


Figure 7-18. DAC Full-Scale Current vs. DAC Gain Code

Transmit DAC Transfer Function

The output currents from the IOUT1P/IOUT2P and IOUT1N/ IOUT2N pins are complementary, meaning that the sum of the two currents always equals the full-scale current of the DAC. The digital input code to the DAC determines the effective differential current delivered to the load. IOUT1P/IOUT2P provide maxi- mum output current when all bits are high. The output currents vs. DACCODE for the DAC outputs are expressed as

$$I_{OUTP} = \left(\frac{DACCODE}{2^N} \right) \times I_{OUTFS}$$

$$I_{OUTN} = I_{OUTFS} - I_{OUTP}$$

where *DACCODE* = 0 to $2^N - 1$.

Transmit DAC Output Configurations

The optimum noise and distortion performance of the B9122RH is realized when it is configured for differential operation. The common-mode error sources of the DAC outputs are significantly reduced by the common-mode rejection of a transformer or differential amplifier. These common-mode error sources include even-order distortion products and noise. The enhancement in distortion performance becomes more significant as the frequency content of the reconstructed waveform increases and/or its amplitude increases. This is due to the first-order cancellation of various dynamic common-mode distortion mechanisms, digital feedthrough, and noise.

Figure 7-19 shows the most basic transmit DAC output circuitry. A pair of resistors, R0, is used to convert each of the complementary output currents to a

differential voltage output, VOUT. Because the current outputs of the DAC are high impedance, the differential driving point impedance of the DAC outputs, ROUT, is equal to 2 × R0.

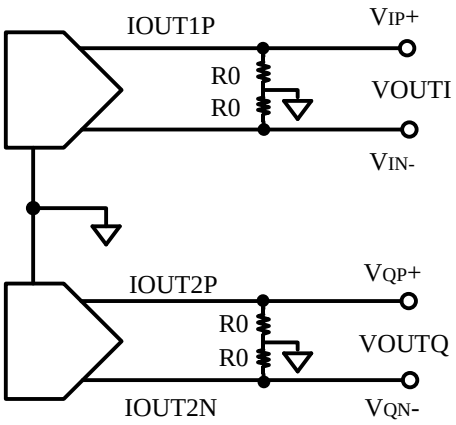


Figure 7-19. Basic Transmit DAC Output Circuit

7.3.4.2 Auxiliary DAC Operation

The B9122RH has two auxiliary DACs: one associated with the I path and one associated with the Q path. These auxiliary DACs can be used to compensate for dc offsets in the transmitted signal. Each auxiliary DAC has a single-ended current that can sink or source current into either the positive (P) or negative (N) output of the associated transmit DAC. The auxiliary DAC structure is shown in Figure 7-20.

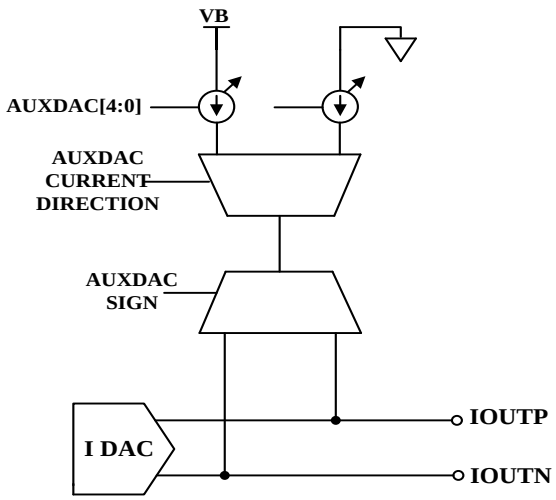


Figure 7-20. Auxiliary DAC Structure

The control registers for the I and Q auxiliary DACs are Register 0x42, Register 0x43, Register 0x46, Register 0x47.

7.3.5 Multichip Synchronization

System demands may require that the outputs of multiple DACs be synchronized with each other or with a system clock. Systems that support transmit diversity or beamforming, where multiple antennas are used to transmit a correlated signal, require multiple DAC outputs to be phase aligned with each other. Systems with a time division multiplexing transmit chain may require one or more DACs to be synchronized with a system-level reference clock.

Multiple devices are considered synchronized to each other when the state of the clock generation state machines is identical for all parts and when time-aligned data is being read from the FIFOs of all parts simultaneously. Devices are considered synchronized to a system clock when there is a fixed and known relationship between the clock generation state machine and the data being read from the FIFO and a particular clock edge of the system clock. The B9122RH has provisions for enabling multiple devices to be synchronized to each other or to a system clock.

The B9122RH supports synchronization in two different modes: data rate mode and FIFO rate mode. In data rate mode, the input data rate represents the lowest synchronized clock rate. In FIFO rate mode, the FIFO rate, which is the data rate divided by the FIFO depth of 8, represents the lowest rate clock.

When the synchronization state machine is on in data rate mode, the elasticity of the FIFO is not used to absorb timing variations between the data source and the DAC, resulting in setup and hold time windows repeating at the input data rate.

The method chosen for providing the DAC sampling clock directly affects the synchronization methods available. When the device clock multiplier is used, only data rate mode is available. When the DAC sampling clock is sourced directly, both data rate mode and FIFO rate mode synchronization are available. The following sections describe the synchronization methods for enabling both clocking modes and querying the status of the synchronization logic.

7.3.5.1 Synchronization With Clock Multiplication

When using the clock multiplier to generate the DAC sample rate clock, the REFCLK input signal acts as both the reference clock for the PLL-based clock multiplier and the synchronization signal. To synchronize devices, distribute the REFCLK signal with low skew to all the devices that need to be synchronized. Skew between the REFCLK signals of the different devices shows up directly as a timing

mismatch at the DAC outputs.

Because two clocks are shared on the same signal, an appropriate frequency must be chosen for the synchronization and REFCLK signals. The FRAME and DCI signals can be created in the FPGA along with the data. A circuit diagram of a typical configuration is shown in Figure 7-21.

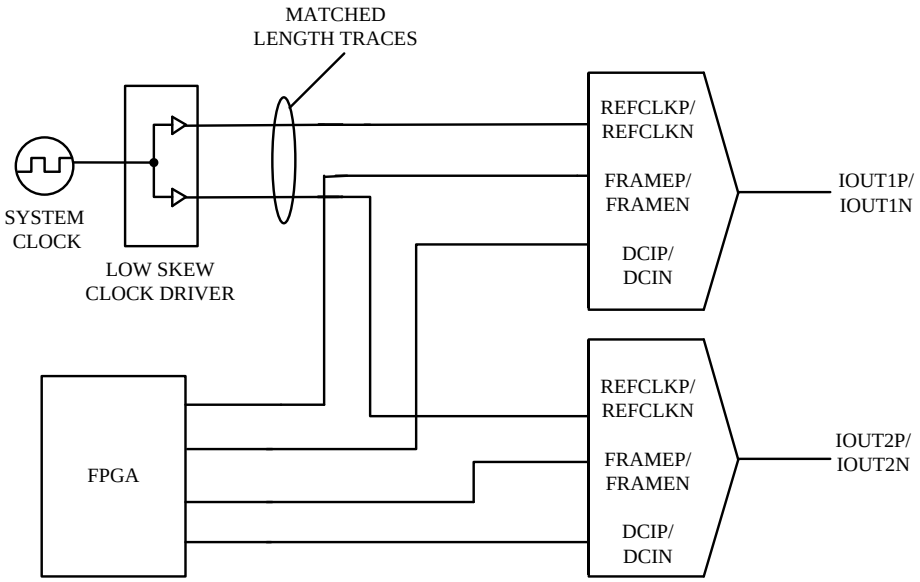


Figure 7-21. Typical Circuit Diagram for Synchronizing Devices

7.3.5.2 Synchronization With Direct Clocking

When directly sourcing the DAC sample rate clock, a separate REFCLK input signal is required for synchronization. To synchronize devices, the DACCLK signal and the REFCLK signal must be distributed with low skew to all the devices being synchronized. If the devices need to be synchronized to amaster clock, use the master clock directly for generating the REFCLK input.

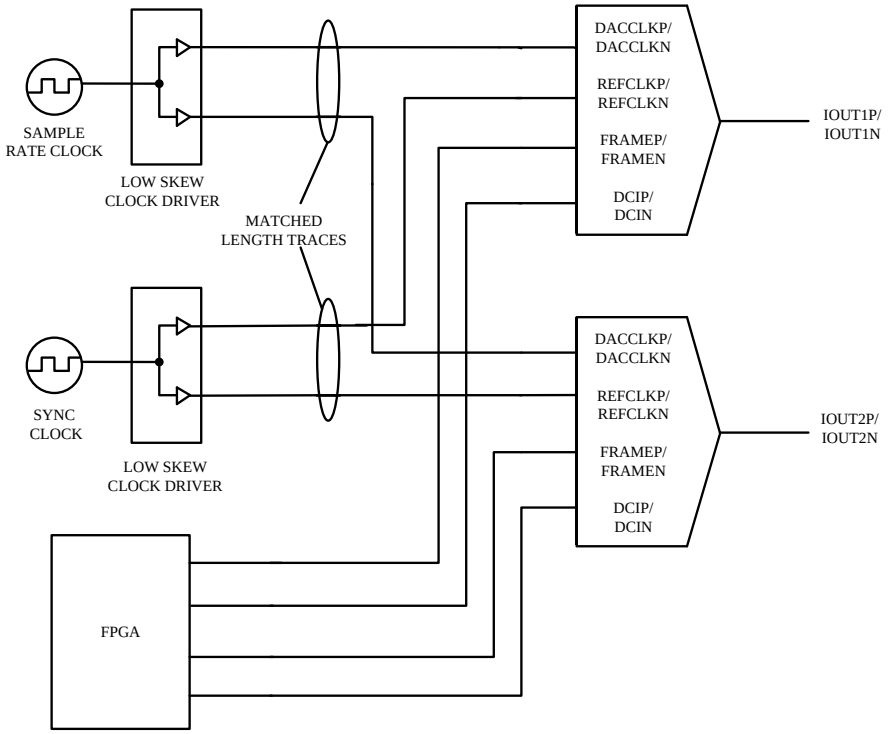


Figure 7-22. Typical Circuit Diagram for Synchronizing Devices to a System Clock

7.3.5.3 Data Rate Mode Synchronization

The Procedure for Data Rate Synchronization When Directly Sourcing the DAC Sampling Clock section outlines the steps required to synchronize multiple devices in data rate mode. The procedure assumes that the DACCLK and REFCLK signals are applied to all the devices. The following procedure must be carried out on each individual device.

Procedure for Data Rate Synchronization When Directly Sourcing the DAC Sampling Clock

Configure the B9122RH for data rate, periodic synchronization by writing 0xC8 to the sync control register (Register 0x10).

Read the sync locked bit (Register 0x12, Bit 6) to verify that the device is back-end synchronized. A high level on this bit indicates that the clocks are running with a constant and known phase relative to the synchronization signal.

Reset the FIFO by strobing the FRAME signal high for one complete DCI period. Resetting the FIFO ensures that the correct data is being read from the FIFO of each of the devices simultaneously.

This completes the synchronization procedure; all devices should now be synchronized.

ensure that each DAC is updated with the correct data on the same CLK edge, two timing relationships must be met on each DAC.

• DCIP/DCIN and D[15:0]P/D[15:0]N must meet the setup and hold times with respect to the rising edge of DACCLK.

• Synchronization (REFCLK) must also meet the setup and hold times with respect to the rising edge of DACCLK.

When these conditions are met, the outputs of the DACs are updated within one DAC clock cycle of each other. The timing requirements of the input signals are shown in Figure 7-23.

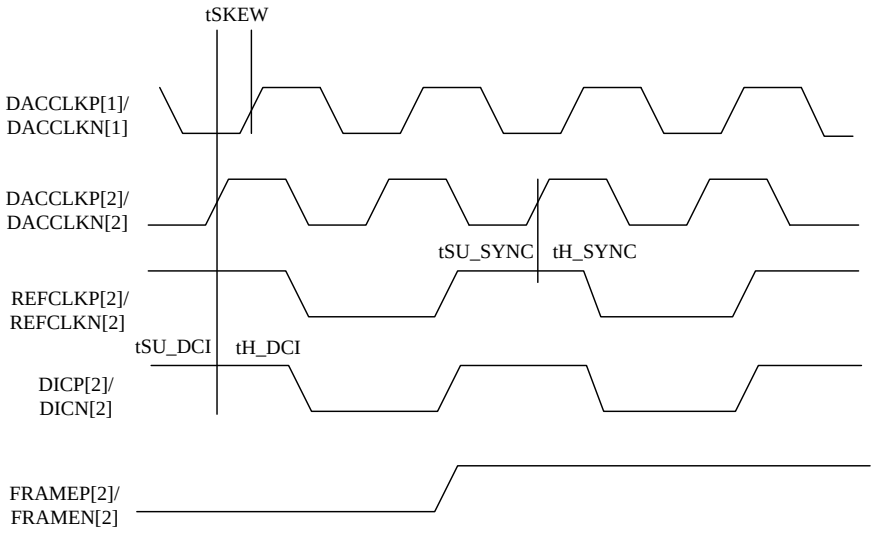


Figure 7-23. Data Rate Synchronization Signal Timing Requirements, 2× Interpolation

Figure 7-23 shows the synchronization signal timing with 2X interpolation; therefore, $f_{DCI} = ½ \times f_{CLK}$. The REFCLK input is shown to be equal to the data rate. The maximum frequency at which the device can be resynchronized in data rate mode can be expressed as

$$f_{SYNC\_I} = f_{DATA}/2^N$$

where N is any non-negative integer.

Generally, for values of N greater than or equal to 3, select the FIFO rate synchronization mode.

When synchronization is used in data rate mode, the timing constraint between the DCI and DACCLK must be met according to Table 7-16. In data rate mode, the allowed phase drift between the DCI and DACCLK is limited to one DCI cycle. The DCI to DACCLK timing restriction is required to prevent corruption of the data transfer when the FIFO is constantly reset. The required timing between the DCI and DACCLK is shown in Figure 7-24.

Table 7-16 DCI to DACCLK Setup and Hold Times

DCI Delay Register 0x16, Bits[1:0]	Minimum Setup Time, t_{SDCI}(ns)	Minimum Hold Time, t_{HDCI}(ns)	Sampling Interval(ns)
00	−0.07	0.82	0.75
01	−0.24	1.13	0.89
10	−0.39	1.40	1.01
11	−0.49	1.55	1.06

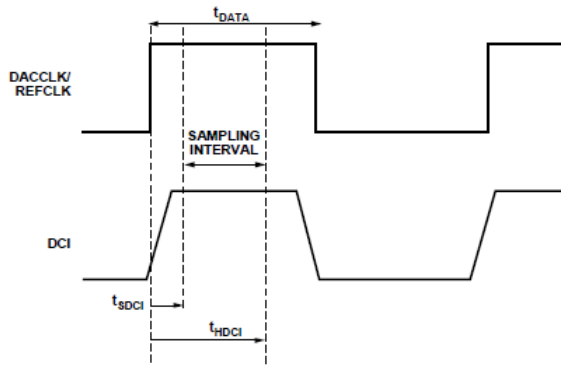


Figure 7-24 Timing Diagram for Input Data Port (Data Rate Mode)

7.3.5.4 FIFO Rate Mode Synchronization

The Procedure for FIFO Rate Synchronization When Directly Sourcing the DAC Sampling Clock section outlines the steps required to synchronize multiple devices in FIFO rate mode. The procedure assumes that the DACCLK and REFCLK signals are applied to all the devices. The procedure must be carried out on each individual device.

Procedure for FIFO Rate Synchronization When Directly Sourcing the DAC Sampling Clock

Configure the B9122RH for FIFO rate, periodic synchronization by writing 0x88 to the sync control register (Register 0x10). Additional synchronization options are available (see the Additional Synchronization Features section).

Read the sync locked bit (Register 0x12, Bit 6) to verify that the device is back-end synchronized. A high level on this bit indicates that the clocks are running with a constant and known phase relative to the synchronization signal.

Reset the FIFO by strobing the FRAME signal high for one com-plete DCI period. Resetting the FIFO ensures that the correct data is being read from the FIFO of each of the devices simultaneously.

This completes the synchronization procedure; all devices should now be synchronized.

When these conditions are met, the outputs of the DACs are updated within one DAC clock cycle of each other. The timing requirements of the input signals are shown in Figure 7-25.

Figure 7-25 shows the synchronization signal timing with 2X interpolation; therefore, f_{DCI} =½×f_{CLK}. The REFCLK input is shown to be equal to the FIFO rate. The maximum frequency at which the device can be resynchronized in FIFO rate mode can be expressed as

$$f_{SYNC\_I} = f_{DATA}/(8 \times 2^N)$$

where N is any non-negative integer.

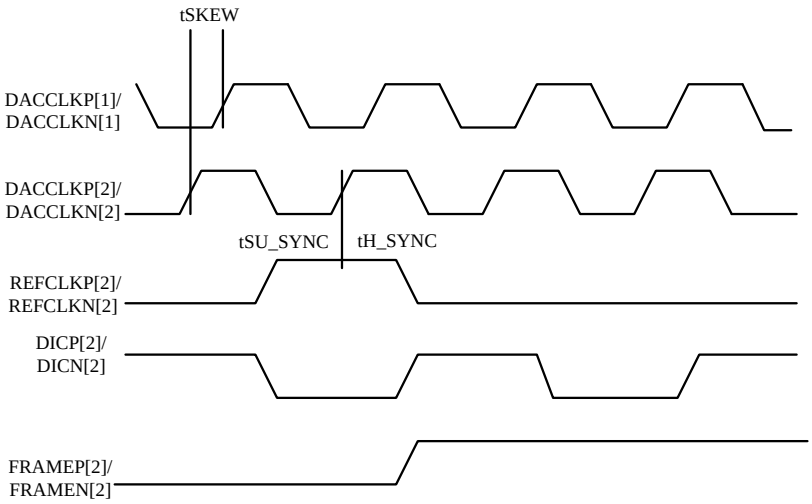


Figure 7-25. FIFO Rate Synchronization Signal Timing Requirements, 2× Interpolation

8. Storage Condition

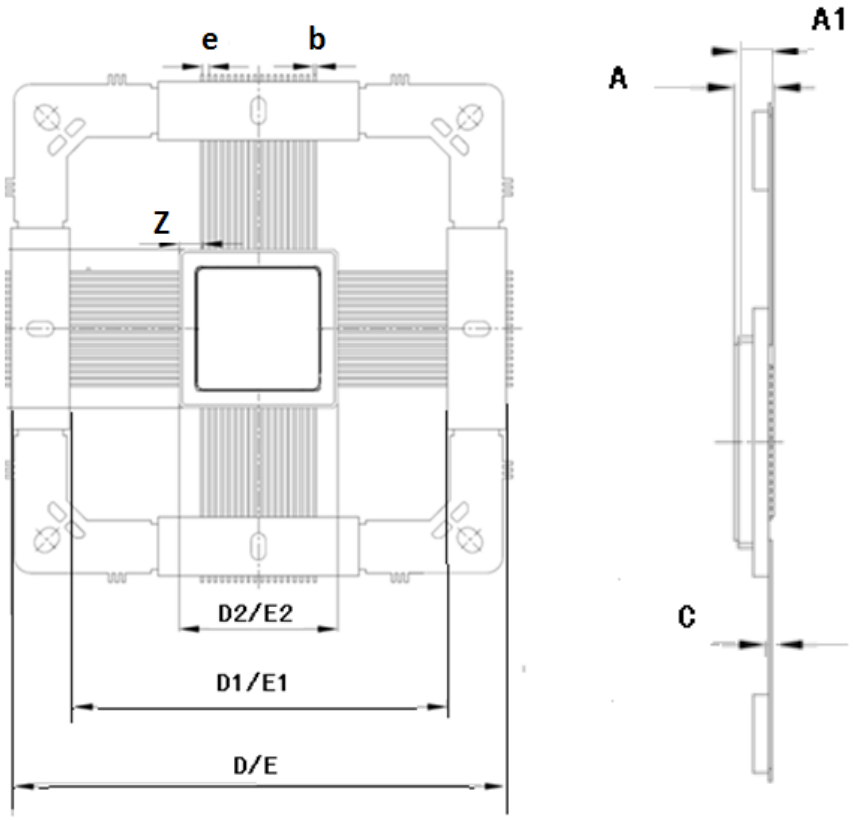
The warehouse environment of B9122RH should be consistent with requirements of the Ⅰ class warehouse, and comply with the requirements of 4.1.1 of "The Space Component's effective storage period and extended retest requirements":

- The device must be stored in a warehouse with good ventilation and no acid, alkaline, or other corrosive gas around. The temperature and humidity should be controlled within a certain range as follow:

The Class of Storage Environment

Symbol	Temperature(℃)	Relative Humidity (%)
Ⅰ	10~25	25~70
Ⅱ	-5~30	20~75
Ⅲ	-10~40	20~85

9. Package Outline dimensions



Symbol	Value（Units：mm）	
	Min.	Max.
A	1.80	2.80
A1	1.30	2.20
b	0.15	0.25
c	0.10	0.20
D/E	36.85	38.05
D1/E1	28.11	29.01
D2/E2	11.55	12.45
e	0.45	0.55
z	1.12	2.33

NOTE: The EPAD Dimension is（8.4±0.15）mm ×（8.4±0.15）mm

Figure 8-1 B9122RH Outline Dimensions

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